Abstract—In this article, a modified hybrid dc breaker and a half-bridge modular multilevel converter (MMC) are employed to interrupt the dc fault current in a high-voltage direct current transmission system. In the hybrid dc breaker, parallel to the main branch, a series connection of an energy-absorbing capacitor and a Thyristor stack is employed. When a dc fault current is recognized, the Thyristor stack is triggered and the load commutation switch in the main branch is turned off. In addition, in the fault clearing state, the MMC is programmed to generate zero voltages at all arms. Using this mechanism, a second-order RLC circuit with zero input is formed, and the fault current is cleared in a very short time. A freewheeling path is provided to bypass the dc line when the equivalent inducement seen from the dc line is large. In contrast to conventional approaches, the peak of dc fault current is limited to a specific limit and the necessity to ultrafast mechanical switches is avoided. In addition, the amplitude of arms currents and corresponding insulated-gate bipolar transistors are kept in the safe operating area. A detailed circuit analysis of the new method is given and design formulas are extracted. Simulation results are provided in PSCAD/EMTDC environment, and experimental results are presented for a scaled-down prototype.

I. INTRODUCTION

RECENTLY, the modular multilevel converter (MMC) has gained more attention for the application of voltage source converter based high voltage direct current (HVdc) transmission systems. This converter is extremely modular, highly efficient, and simply scalable to higher voltage ratings [1]. The conventional MMC, which employs half-bridge submodules (known as HB-MMC), is preferred for HVdc applications because it needs the minimum number of components and has the lowest amount of power losses. The HB-MMC, however, is vulnerable to dc-side short-circuit pole-to-pole (or pole-to-ground) faults and is not able to block the dc fault current [2]. The short-circuit current that flows through the semiconductor devises for several milliseconds will increase the junction temperature significantly and may cause the device failure.

Due to the weakness of HB-MMC against dc fault currents, this converter is usually employed in applications where cable transmission is preferred [3]. To overcome the weakness of HB-MMC and to extend its application to overhead transmission lines, two approaches have been introduced in the literature [4]. The first method is based on employing dc breakers in transmission systems. But in contrast to ac systems, there is no natural zero point in dc currents, and the mechanical switches cannot interrupt the fault current [2]. There are some methods that employ resonant elements to form resonant circuits after a dc fault and to interrupt the fault current by mechanical switches [5]. These schemes generally need 20–40 ms (or 8–10 ms) for the fault interruption in passive (or active) resonant modes, respectively [6]. A fully semiconductor-based dc breaker can also interrupt the fault current in a very short time. But this method needs a high number of series devices in the main branch and causes significant power losses in normal operating conditions. To overcome the weaknesses of mechanical switches and semiconductor-based dc breakers, the hybrid dc breakers have been introduced [7]. They offer very low conduction losses and can interrupt the dc fault current in a very short time.

The second approach to interrupt the dc fault current is based on MMC topologies with dc fault current blocking capability [8]–[13]. These topologies employ bipolar submodules (SMs) such as full-bridge, semi full-bridge, and cross-connected [8], [9] or asymmetric SMs such as unidirectional full-bridge and clamped-double [10], [11] in their arms. Some newer topologies employ hybrid arm structures [12], [13], where one arm is fully HB and the second arm is made of bipolar (or asymmetric) SMs to prevent overvoltages on the MMC switches under ac-side phase-to-ground faults [14]. In all of these configurations, when a dc fault is recognized, the converter is programmed to the blocking mode and IGBTs are turned off. Then counter electromotive force (EMF) voltages are inserted by bipolar or asymmetric SMs in MMC arms and the fault current is interrupted in a very short time.
From the engineering point of view, when a hybrid dc breaker is employed for the protection of HB-MMC, the losses will be the minimum possible value. Also, after a dc fault, the hybrid dc breaker can isolate the faulty line from rest of the network [15], a very interesting feature for operation in dc grids. On the other side, MMCs with dc fault blocking capability have higher losses compared to the first approach. Also, during a dc fault, all MMCs should stop working for several milliseconds which will cause the power flow interruption in the whole transmission system [16]. Due to these limitations, the focus of this article will be on the integration of hybrid dc breaker with the HB-MMC for HVdc transmission systems.

The existing hybrid dc breakers employ a series combination of ultrafast disconnector (UFD) and the load commutation switch (LCS) in the main branch of the breaker. Also, a stack of IGBTs is used in the parallel branch to break the dc fault current [7]. An alternative approach is using several Thyristor stacks with series-connected capacitors in parallel to the main branch [17]. In both of these approaches, a stack of metal oxide varistors (MOVs) or voltage arresters is needed parallel to the hybrid dc breaker to generate enough counter-EMF (at least 1.5 times of the nominal dc-link voltage) to interrupt the fault current and to dissipate the fault energy. Any delay in the opening of UFDs will cause higher current levels and higher stress on MMC switches and the breaker elements. Hence, to control the slope of fault current in these breakers, large dc reactors are used in series with the breakers, which may cause voltage instability problem in dc grids [18]. Liu et al. [19] have employed a Thyristor controlled resistor in parallel to the dc reactor and inserts it to the circuit in the fault period. This strategy helps to reduce the stress on MOVs and to accelerate the fault current interruption. Song et al. [20] have proposed a different methodology, where it generates zero voltages at MMC arms in the fault period and stores the converter-side and line-side energies in two energy-absorbing capacitors. In this approach, the LCS tolerates a voltage equal to the sum of capacitors voltages and it may reach 10% of the dc-link voltage. Using this method, the semiconductor breaker and the parallel arrester are eliminated and the current stress is reduced. But, on the other side, more number of IGBTs are needed in the LCS configuration, which increases the losses in the normal operation. In addition, during the fault current interruption, there is no control on the arms currents and the IGBTs currents may exceed the safe operating area.

In this article, a new circuit of hybrid dc breaker with the fault current interruption strategy in [20] is introduced. The proposed circuit employs a series connection of the Thyristor stack and the energy-absorbing capacitor parallel to the main branch. In contrast with [20], less number of components are used and the voltage of LCS is limited to 5% of the dc-link voltage. Moreover, the amplitude of arms currents is controlled and the MMC IGBTs are kept in the safe operating area. Using the proposed method, the slower mechanical disconnector can be used and there is no need to MOV stacks. The design formulas are presented and the validity of the new approach is verified by simulations in PSCAD/EMTDC environment. In addition, experimental results are provided for a scaled-down prototype.

**II. TOPOLOGY OF THE HYBRID DC BREAKER**

In this section, first the topology of conventional hybrid dc breaker (proposed by ABB) is introduced and then the proposed structure is explained.

**A. Topology of Conventional Hybrid dc Breaker**

The topology of the proposed hybrid dc breaker in [7] is shown in Fig. 1. This topology has two branches: the main current path and the semiconductor breaker path. The main branch includes an ultrafast mechanical disconnector known as UFD and a semiconductor switch known as LCS. During the normal operation of the HVdc system, the dc current flows through the main path and the conduction losses are very low. When a pole-to-ground fault happens, the semiconductor breaker is turned on and the LCS in the main branch is turned off. This action causes the dc current to commutate completely to the semiconductor breaker. Then, a turn-off command is sent to the UFD. After almost 2 ms, the UFD is opened and the semiconductor breaker is turned off. Next, the stored energy in inductors and the dc line are dissipated by MOVs in a very short time and the fault current falls to zero. In this method, a large dc reactor is needed in series with the breaker to limit the rise of fault current in the fault period; otherwise, the fault current may reach large values and the stress on semiconductor switches and MOVs will be high. In addition, the stored energy in the dc reactor must be dissipated by MOVs in a very short time.

**B. Topology of Proposed Hybrid DC Breaker**

In Fig. 2, the topology of the proposed hybrid dc breaker is shown. This structure uses a series connection of a Thyristor...
valve $T_1$ and an energy-absorbing capacitor $C_1$, instead of the semiconductor breaker and the MOV arrester. After opening of the hybrid dc breaker, a freewheeling path is formed at the dc line by the freewheeling diode $D_1$ and the series capacitor $C_2$. The employed resistors $R_1$ and $R_2$ (parallel to capacitors $C_1$ and $C_2$) will dissipate the fault energy. But, in contrast to [7], the energy can be dissipated in a longer time, e.g., $0.1–0.2$ s.

In the proposed circuit of Fig. 2, both the MMC station and the hybrid dc breaker react simultaneously to interrupt the fault current. In other words, when a dc-side short-circuit fault happens, the dc-link current $i_d$ rises quickly and reaches the trip level $I_f$. Then, the MMC is programmed to generate zero voltages at all arms and the hybrid dc breaker is controlled in four steps to interrupt the fault current. In contrast to [7] and [20], ac-side reactors $L_f$ are also employed to control the amplitude of arms currents in the fault clearing period. In the proposed method, the duration of fault current interruption, the amplitude of arms currents, and the LCS voltage are important factors, which are investigated in Section III.

### III. OPERATING PRINCIPLE OF NEW HYBRID BREAKER

In this section, the operating principle of the new hybrid dc breaker is presented. For this article, the simplified model of MMC and the breaker are shown in Fig. 3. One should note that the set of dc line and the short-circuit path is modeled by an equivalent inductance $L_{dc}$ and a resistance $R_{dc}$. To understand the operating principle of the new method, it is assumed that the pole-to-ground fault occurs at $t = t_o$ and the following procedure is taken to interrupt the fault current. Also, the key waveforms, including the dc-line current ($i_d$), the MMC dc-link current ($i_d$), the LCS current ($i_{LCS}$), the Thyristor current ($i_1$), the freewheeling diode current ($i_2$), and the Thyristor voltage $v_t$ are shown in Fig. 4, respectively.

1) **During** $t_o–t_1$: The current $i_d$ rises quickly as a function of $V_d/(L_{dc} + 2/3L_a)$, where $V_d$ is the nominal dc-link voltage and $L_a$ is the arm inductance. At $t = t_1$, the dc current reaches the trip level $I_f$, which is set to be two times the rated dc-link current and the fault signal is generated.

2) **During** $t_1–t_2$: After generation of fault signal at $t = t_1$, the Thyristor stack $T_1$ is triggered and the MMC is programmed to generate zero voltages at its arms. In other words, all bottom switches in the MMC SMs are turned ON [the simplified model is shown in Fig. 3(a)]. This action isolates ac-side sources from the dc-side fault point and prevents the discharge of SMs capacitors. Accordingly, the rise of dc-link current $i_d$ is prevented and the fault energy is limited. Due to lower turn-on resistance of LCS branch, the main part of dc-link current $i_d$ is passing through it. In addition, during the time interval $t_1–t_2$, it is possible to communicate with other protective devices and decide whether the fault is real or not. After the fault confirmation, the LCS is turned OFF at $t = t_2$, and the current $i_{LCS}$ is commutated to the Thyristor path.

3) **During** $t_2–t_3$: After LCS turn-OFF and current commutation, the turn-OFF command is sent to MD. Simultaneously, the current $i_1$ charges the capacitor $C_1$ and by the voltage increase $v_1$, the current $i_1$ reduces. However, the line current $i_L$ does not reduce with the same rate as $i_1$ (this assumption is valid when $L_{dc} \gg L_a$ and $R_{dc}$ is small). As a result, the current $i_2 = i_L - i_1$ passes through the freewheeling diode $D_1$. Since then, a second-order RLC circuit with zero input source is formed at the left loop of Fig. 3(b) and $i_2$ falls to zero quickly. This operating state is ended when the current $i_d$ becomes zero and $T_1$ is naturally turned OFF.

4) **During** $t_3–t_4$: During this time interval, the negative voltage ($-v_1$) is applied to the Thyristor stack $T_1$, which guarantees its correct turn-OFF. Furthermore, the opening of mechanical disconnector is completed at $t = t_4$. Since then, the faulty line is isolated from the MMC station and the MMC IGBTs can be turned OFF or they can be controlled to exchange reactive power with the ac grid. One should note that for $t > t_4$, the equivalent circuit in Fig. 3(b) is no longer valid and Fig. 3(c) is used for the rest analysis.

![Fig. 3](image-url)
Finally, the capacitors $C_1$ and $C_2$ are discharged by parallel resistors $R_1$ and $R_2$. It is worth noting that when a pole to ground fault happens, an arc is formed and this arc provides a path to ground for the dc current. The common practice in overhead lines is to bring the dc current down to zero and wait for a predetermined time (known as de-energized or deionization time) in order to allow the arc to extinguish and the ionised air to disperse [3]. Typically, the waiting time is around 0.2–0.5 s [3, 22]. In this article, the resistors $R_1$ and $R_2$ are selected to discharge $C_1$ and $C_2$ in about 0.1 s and afterward the hybrid dc breaker can reclose.

A. Circuit Analysis of the Proposed Structure

To simplify the circuit analysis in the fault interruption period, the following assumptions are considered.

1) Three-phase ac-side voltage is balanced.
2) All switches and diodes are assumed to be ideal.
3) Discharging effect of $R_1$ and $R_2$ is ignored during $t_1 \rightarrow t_4$.
4) “Fault confirmation” interval is ignored, i.e., $t_2-t_1 = 0$.
5) $t = t_2$ is considered as the time origin for calculations.

Based on circuit analysis and explanations in Section IV-C, the worst case operating condition is related to the situation that the equivalent inductance seen from the line side $L_{eq}$ is much greater than $L_a$ and the equivalent resistance seen from the line side $R_{eq}$ is very small (or close to zero). Then, for the short period of $t_1 \rightarrow t_3$, one can assume a constant current behavior for the line-side inductance, i.e.,

$$i_L(t) \approx i_d(t_1) = I_f \quad (t_1 \leq t < t_3). \quad (1)$$

Next, in Fig. 3(b), by writing KVL for the loop containing $C_1$, $C_2$, and one leg of MMC, one can derive

$$L_a \frac{di_{xu}}{dt} + L_a \frac{di_{xl}}{dt} = v_2 - v_1, \quad x = a, b, c \quad (2)$$

where, $i_{xu}$ is the upper arm current in the leg $x$ ($x = a, b, c$), $i_{xl}$ is the lower arm current in that leg, $v_1$ is the voltage of $C_1$, and $v_2$ is the voltage of $C_2$. By summing (1) for three legs of MMC and noting to the following KCL:

$$i_{au} + i_{bu} + i_{cu} = i_{ai} + i_{bi} + i_{ci} = i_d = i_1 \quad (t_2 \leq t < t_3) \quad (3)$$

the following result is obtained:

$$L_a \frac{di_1}{dt} = 1.5(v_2 - v_1). \quad (4)$$

Also, the following KCL is written for the line-side node:

$$i_1 + i_2 = i_L(t) \approx I_f \quad (t_2 \leq t < t_3) \quad (5)$$

where, $i_1$ and $i_2$ represent the capacitors currents and are related to $v_1$ and $v_2$ as follows:

$$i_1 = C_1 \frac{dv_1}{dt}, \quad i_2 = C_2 \frac{dv_2}{dt}. \quad (6)$$

Now from (4), (5), and (6), and noting to the initial conditions of capacitors at $t = t_2$, i.e., $v_1(t_2) = v_2(t_2) = 0$, the following equations are derived for the MMC dc-side voltage and current:

$$v_d = v_1 - v_2 = \frac{I_f}{C_1 \omega_o} \sin(\omega_o t) \quad (7)$$

$$i_d = i_1 = \left(\frac{C_2}{C_1 + C_2} \cos(\omega_o t) + \frac{C_1}{C_1 + C_2}\right) I_f \quad (8)$$

where

$$\omega_o = \sqrt{\frac{(C_1 + C_2)}{L_1 C_1 C_2}}, \quad L_1 = \frac{2}{3} L_a. \quad (9)$$

One important variable is the LCS voltage, which is equal to $v_1$ in the time interval $t_2 \rightarrow t_3$. Hence, the variable $v_1$ is calculated by integration over $i_1$, i.e.,

$$v_1 = \frac{I_f}{C_1} \left(\frac{C_2}{C_1 + C_2} \sin(\omega_o t) + \frac{C_1}{C_1 + C_2} t\right) \quad (10)$$

and the voltage of LCS is obtained as

$$v_{LCS} = \frac{I_f}{C_1} \left(\frac{C_2}{C_1 + C_2} \sin(\omega_o t) + \frac{C_1}{C_1 + C_2} t\right), \quad t_2 \leq t < t_3. \quad (11)$$

Also, the required time for clearing the fault current can be obtained from (8) as follows:

$$i_d = 0 \rightarrow t_{clr} = t_3 - t_2 = \frac{1}{\omega_o} \cos^{-1}\left(\frac{C_1}{C_2}\right) \quad (12)$$

where $t_{clr}$ shows the required time for $i_d$ to reach zero value. From (12), one can conclude that the capacitance value $C_1$ must be selected lower than $C_2$ to have a solution for (12). Also, the evaluation of (11) and (12) shows that the variables $v_{LCS}$ and $t_{clr}$ are minimum when $C_1 < < C_2$, i.e.,

$$v_{LCS} \leq \sqrt{L_1/C_1} I_f \quad \text{when } C_1 \leq C_2 \quad (13)$$

$$t_{clr} \approx \frac{\pi}{2} \sqrt{L_1 \cdot C_1} \quad \text{when } C_1 \leq C_2. \quad (14)$$
In practice, choosing $C_2$ five times greater than $C_1$ is enough to satisfy the operating conditions in (13) and (14). Another important criterion for the design of the proposed system is the maximum arms currents in the fault clearing period. To calculate the arms currents, the following KVL is written at the ac side of MMC and the lower arm:

$$v_{xn} + v_{no} = L_f \frac{di_x}{dt} - L_a \frac{di_{xl}}{dt}, \quad x = a, b, c$$

(15)

where $v_{xn}$ represents phase-x voltage and $v_{no}$ is the voltage of neutral point to the bottom link of MMC. Through summation of (15) for three phases and noting that $i_a + i_b + i_c = 0$, one can derive the following relation:

$$v_{no} = \frac{-1}{3L_a} \frac{di_1}{dt}.$$

(16)

Now by inserting $v_{no}$ value from (16) into (15) and ($v_{2} - v_{1}$) from (4) into (2), and noting to the KCL relation at the ac terminal of MMC, the following equations are derived:

$$\begin{align*}
v_{xn} - \frac{1}{3L_a} \frac{di_{1}}{dt} &= L_f \frac{di_x}{dt} - L_a \frac{di_{xl}}{dt} \\
L_a \frac{di_x}{dt} + L_a \frac{di_{xl}}{dt} &= 2L_a \frac{di_1}{dt}, \quad x = a, b, c.
\end{align*}$$

(17)

From the relations in (17) and with some mathematical calculations, the following equations are derived for the upper and lower arms currents:

$$\begin{align*}
&\left\{ \begin{align*}
    i_{xu} = i_{xu}(t_1) + \frac{1}{2(L_f + L_a/2)} \int_{t_1}^{t} v_{xn} dt \\
    \frac{1}{3} C_n \omega S L_f \left( 1 - \cos(\omega t) \right)
\end{align*} \right.
\end{align*}$$

(18)

$$\begin{align*}
&\left\{ \begin{align*}
    i_{xl} = i_{xl}(t_1) - \frac{1}{2(L_f + L_a/2)} \int_{t_1}^{t} v_{xn} dt \\
    -\frac{1}{3} C_n \omega S L_f \left( 1 - \cos(\omega t) \right)
\end{align*} \right.
\end{align*}$$

(19)

and initial values $i_{xu}(t_1)$ and $i_{xl}(t_1)$ can be obtained as

$$\begin{align*}
    i_{xu}(t_1) &\approx \frac{i_{xu}(t_1)}{3} + \frac{i_{xu}(t_1)}{2} = \frac{i_{xu}(t_1)}{2} + \frac{i_{xu}(t_1)}{2} \\
    i_{xl}(t_1) &\approx \frac{i_{xl}(t_1)}{3} - \frac{i_{xl}(t_1)}{2} = \frac{i_{xl}(t_1)}{3} - \frac{i_{xl}(t_1)}{2}
\end{align*}$$

(20)

where $i_x$ is phase-x current. By assuming that the phase-x voltage has the form of $v_{xn} = V_m \sin(\omega t + \theta_x)$ and $C_1 < < C_2$, (18) is simplified as

$$\begin{align*}
&\left\{ \begin{align*}
    i_{xu} = i_{xu}(t_1) + \frac{I_f \cos(\omega t)}{3} + \frac{V_m \cos(\omega t + \theta_x)}{2(L_f + L_a/2)} \\
    i_{xl} = i_{xl}(t_1) - \frac{I_f \cos(\omega t)}{3} - \frac{V_m \cos(\omega t + \theta_x)}{2(L_f + L_a/2)}
\end{align*} \right.
\end{align*}$$

(21)

where $V_m$ is the peak of phase voltage, $\omega$ is the grid angular frequency, and $\theta_x$ is the phase-x voltage angle. During fault clearing period, the arms currents change according to (20) and may reach the maximum value. In continue, the maximum arms currents are calculated by considering that the fault current is cleared in less than 5 ms ($t_3 - t_1 < 5$ ms) and the opening time of MD is 5 ms.

To find the maximum arms currents in (20), $i_x(t_1)$ is approximated by $I_m$, where $I_m$ shows the peak of rated phase current. Also, the second term in (20) is ignored since it reduces continuously and becomes zero at $t = t_1$. Finally, the numerator of the third term in (20) is approximated by $\sqrt{2V_m}$ to obtain the maximum value. Considering all these points, the maximum arms currents in the worst-case operating condition can be obtained as

$$I_{arm,max} = \max(I_{xu}, I_{xl}) \approx \frac{I_m}{2} + \frac{\sqrt{2V_m}}{2(L_f + L_a/2)}$$

(22)

where $I_{arm,max}$ is the maximum arm current in worst-case condition. From (21), it is evident that the peak of the arm current can be limited by $L_f$ in the fault period.

### B. Design Methodology of Proposed Circuit

Using (13), (14), and (21), one can determine the main parameters of the hybrid dc breaker. To achieve this goal, the following parameters are defined at first:

1. $I_f$ or the trip level of fault current;
2. $t_{clr}$ or the desired time for clearing the fault current;
3. $V_{lcs,max}$ or the upper limit of LCS voltage;
4. $I_{arm,max}$ or the peak current in arms and IGBTs.

First, the arm inductance is determined from (13) and (14)

$$L_a = \frac{3}{2} L_1 = \frac{3 \times V_{lcs,max} t_{clr}}{I_f}$$

(23)

and the capacitance $C_1$ and $C_2$ are determined as

$$C_1 = \frac{\beta^2 I_f}{L_a t_{clr}^2}, \quad C_2 = 5C_1.$$  

(24)

Next, the ac-side inductor $L_f$ is determined. This value is obtained by comparing the maximum arm current $I_{arm,max}$ in (21) with the maximum transient (or pulse) current that is tolerated by MMC IGBTs in the fault clearing state, i.e.,

$$I_{arm,max} \leq I_{Cpuls}$$

where $I_{Cpuls}$ represents the maximum pulse current of the IGBTs. To determine $I_{Cpuls}$, one has to select the proper IGBT at first. In MMC application, the relationship between the peak arm current in normal operation $I_{arm}$ and the nominal IGBT collector current $I_{Cnom}$ is described by an empirical equation [23]

$$I_{Cnom} \approx \frac{I_{arm}}{\beta} = \left( \frac{I_d}{3} + \frac{I_m}{2} \right) / \beta = \left( \frac{I_d}{3} + \frac{S}{3V_m} \right) / \beta$$

(25)

where $I_d$ is the nominal dc-link current and $S$ is the rated apparent power of the MMC. In (25), $\beta$ is a design factor ($\beta = 1.0 \sim 1.2$) and is selected based on power dissipation and temperature rise of IGBTs [23]. This factor is set to 1.0 in this article. After calculation of $I_{arm}$ in (25), the proper IGBT is selected from the existing high-voltage IGBTs. Then, from (21) and knowing the IGBT type and its peak pulse current, $L_f$ is calculated as

$$L_f \geq 2\omega \left( \frac{\sqrt{2V_m}}{I_{Cpuls} - \frac{S}{3V_m}} - \frac{L_a}{2} \right).$$

(26)

Finally, the parallel resistors $R_1$ and $R_2$ are selected based on the following formulas to dissipate the fault energy in 0.1 s:

$$R_1 \leq \frac{0.1 \omega t_{clr}}{5C_1}, \quad R_2 \leq \frac{0.1 \omega t_{clr}}{5C_2}.$$  

(27)
It is worth noting that in the conventional designs, arm inductors are used to limit the fault current during a dc-side fault and to suppress the circulating current [24]. In this article, the fault current is kept less than the trip level \( I_f \) and it reduces immediately after applying the proposed method. This feature allows the elimination of dc-side reactors and using smaller reactors in MMC arms. Also, by applying the circulating current suppression control [25], the low-frequency circulating current is effectively reduced, and the arm inductance requirement is largely decreased [24].

About \( L_f \) inductors and their size, one should note that the MMC station is connected to the ac system by a Y/Δ transformer. This transformer has a per unit reactance, which may lie in the range 0–0.35 p.u. [26]. In the proposed method, selecting a Y/Δ transformer with a large reactance is beneficial. Also, one has to subtract the equivalent ac inductance (which is the sum of source, line, and transformer inductance) from the \( L_f \) value and to employ the difference in practice. Furthermore, according to (26), a tradeoff can be done between \( L_f \) and \( I_{C\text{puls}} \) to choose a smaller value for \( L_f \) if it is desirable. The last point, but not the least: the voltage (phase) sensors for the control system are located at the connecting points of \( L_f \) inductors to the ac system. Hence, the voltage drop and reactive power consumption of \( L_f \) inductors are compensated by the MMC in most operating points, which is shown in Fig. 10.

### IV. Simulation Results and Comparison

In this part, simulation results are provided to verify the behavior of the proposed integrated hybrid dc breaker. The simulations are carried out at the switch level in PSCAD/EMTDC environment. The parameters of the studied system are shown in Table I. In this article, the hybrid dc breaker is designed to clear the dc fault current in 4 ms and the opening time of mechanical disconnector is set to 5 ms. Also, 0.5 ms is considered for the “fault confirmation.” Furthermore, the LCS voltage is limited to 4% of the dc-link voltage. The rest design parameters are shown in Table II, and the calculated parameters of the system are given in Table III. It is worth noting that according to (25) and Table I, \( I_{C\text{nom}} \approx I_{\text{arm}} = 1.18 \text{ kA} \) and to satisfy (24), 1.2-kA IGBTs are selected for HB-MMC and \( I_{C\text{puls}} \) would be 2.4 kA [27].

#### A. Verification of the Hybrid DC Breaker

In the first simulation, the general behavior of the designed hybrid dc breaker is verified. It is assumed that the system is working at the nominal operating condition and a pole-to-ground fault happens at \( t = 0.3 \text{ s} \). The short circuit path is modeled with \( L_{sc} = 0.1 \text{ H} \) and \( R_{sc} = 0.5 \text{ Ω} \). The corresponding waveforms of dc-link voltage \( v_d \), the dc-link current \( i_d \), and the arm currents \( i_{\Delta\text{u}}, i_{\Delta\text{d}}, i_{\text{abc,u}}, \text{and } i_{\text{abc,d}} \) when a fault occurs at \( t = 0.3 \text{ s} \) and IGBTs with \( I_{C\text{nom}} = 1.2 \text{ kA} \) are employed.

![Main waveforms of the proposed integrated hybrid dc breaker](image-url)
over $C_1$, and the voltage over $C_2$ at the fault interruption period are shown in Fig. 6.

According to Fig. 5, the dc-link current $i_d$ remains lower than $I_f = 2\, \text{kA}$ in the fault clearing period. Also, the demonstrated arms currents $i_{xu}$ and $i_{xl}$ well satisfy the defined condition in (24), i.e., $I_{arm,max} \leq I_{Cpuls} = 2.4\, \text{kA}$.

Fig. 6 verifies the operating principle of the proposed fault clearing method. At $t_1 = 0.3008\, \text{s}$, the dc-link current reaches $I_f = 2\, \text{kA}$ and the fault signal is generated. Then, the MMC is commanded to generate zero voltages at all arms and the Thyristor valve is triggered. Also, the protection system waits 0.5 ms to verify the fault existence. After the fault confirmation, the LCS opens at $t_2 = 0.3013\, \text{s}$, and its current is commutated to the Thyristor path. Then, the mechanical disconnector is commanded to open. Simultaneously, due to formation of second-order circuit with zero input source, the dc-link current $i_d$ falls to zero at $t_3 = 0.3056\, \text{s}$. Finally, with the complete opening of MD at $t_4 = 0.3065\, \text{s}$, the MMC IGBTs are turned OFF.

From the obtained results, it is seen that the time difference $(t_3-t_2)$ is 4.3 ms and is very close to the design goal $t_{cl}=4\, \text{ms}$. The small difference is related to the discharging effect of parallel resistor $R_1$ and can be compensated by decreasing the $C_1$ value. In addition, the maximum LCS voltage is 5.0 kV and well satisfies the design goal, $V_{lcs,max}=6\, \text{kV}$. One should note that the opening time of MD can be selected greater than 5 ms while the system requirements are met.

**B. Comparison With Alternative Hybrid DC Breakers**

The second simulation compares the behavior of new hybrid dc breaker with the proposed hybrid breaker in [7] and the most recent approach in [20]. All three breakers are designed for the same operating condition in Table I. However, for the hybrid dc breaker in [7], one extra 100-mH dc reactor is employed in series with the breaker to limit the current rise; and the opening time of UFD is set to $t_{op}=2.5\, \text{ms}$. Also, the MOV arrester is selected to generate $1.5\, V_d$ during fault current interruption. Hence, the fault clearance time is determined by the system parameters and is different from the two other methods. The comparison results of the three methods are given in Fig. 7.

According to Fig. 7(a), the proposed method in this article and the approach in [20] interrupt the fault current in about 4 ms
nominal operating condition, when the active power is $P = \ldots$ example, the total semiconductor losses of the HB-MMC at the worst case operating condition. But when $L_{sc}$ is much greater than 0.4Ω, and $R_{sc}$ is small, the freewheeling diode $D_1$ starts to conduct at $t = t_2$ and the $i_d = i_1$ path is formed by $L_1$, $C_1$, and $C_2$. This scenario was already discussed in Section III-B as the worst case operating condition. But when $L_{sc}$ and $R_{sc}$ have small values, the freewheeling diode $D_1$ remains off and the $i_d$ path is formed by $L_1$, $C_1$, and $R_{sc}$. Finally, in cases that both $L_{sc}$ and $R_{sc}$ are not small, the freewheeling diode $D_1$ will conduct with some delay (with respect to $t_2$) and the circuit configuration will change between two above extremum cases. In continuation, the corresponding current waveforms at different $L_{sc}$ and $R_{sc}$ values are shown in Fig. 8(b) for the considered case study.

From Fig. 8(b), one can see that the dc-link current $i_d$ falls to zero in almost 4 ms in extremum cases, and less than 4 ms in other cases. Also, the worst case operating condition is related to the right waveform in Fig. 8(b), where $L_{sc} = 100$ mH and $R_{sc} = 0.5Ω$.

Second technical issue is related to the applicability of the presented hybrid dc breaker in multiterminal dc networks. In such networks, the breaker must be able to quickly isolate the faulty line in the dc grid before the MMCs are blocked and power transmission is interrupted. To achieve this goal, dc reactors are needed at both ends of dc lines to minimize the disturbance on the healthy parts of the dc network. This solution has already been introduced for alternative dc breakers in multiterminal networks [28], [29].

In this investigation, the sample multiterminal dc network in Fig. 9(a) with $L_{dc} = 200$ mH is considered. Here, MMC1 is delivering 0.5 p.u. active power to Line-12 and 0.5 p.u. to Line-13. Also, MMC2 is receiving 0.5 p.u. active power from Line-12 and 0.5 p.u. from the other line. At $t = 0.6$ s, a dc fault is considered in Line-13 with $L_{sc} = 0.2$ H and $R_{sc} = 0.5Ω$. Once the dc fault is detected, MMC1, MMC3, and breakers B13 and B31 react to interrupt the fault current and isolate the faulty line, while the rest MMCs and breakers will continue their operation. Also, after separation of faulty line, MMC1 and MMC3 will return to normal operation. Fig. 9(b) shows the corresponding dc terminal voltage of MMC1 and MMC2, the
Fig. 9. Evaluation of proposed method in a multiterminal dc network when a pole-to-ground fault occurs in line-13 at \( t = 0.6 \) s. (a) Sample multiterminal network. (b) Corresponding key waveforms.

From Fig. 9(b), one can see that the arms currents in MMC1 and MMC2 remain lower than 2 p.u., respectively. In other words, the IGBTs remain in safe operating area and MMC converters can continue their operation without blocking. Furthermore, the dc-link voltage of MMC2 reduces to 0.8 p.u. during such severe fault condition and restores in less than 0.1 s.

Third technical issue is related to adoption of ac-side inductors and their effects on the operating area (PQ chart) of MMC in the steady state. To obtain the PQ chart, one has to consider the phasor diagram of the MMC in normal operation. Then, based on phasor theory, the amplitude of synthesized voltage by the sending power by MMC1 (\( P_{dc1} \)), the power in Line-12 (\( P_2 \)), the power in faulty line, and the measured power in ac side of MMC2 (\( P_{ac2} \)). Also upper arms currents \( i_{abc,u} \) in MMC1 and MMC2 are shown to verify their transient behavior.

From Fig. 9(b), one can see that the arms currents in MMC1 and MMC2 remain lower than 2 p.u., respectively. In other words, the IGBTs remain in safe operating area and MMC converters can continue their operation without blocking. Furthermore, the dc-link voltage of MMC2 reduces to 0.8 p.u. during such severe fault condition and restores in less than 0.1 s.

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\[
|V'_{\phi}| = \sqrt{|V_{\phi n}|^2 + X^2 |I|_\phi^2 + 2X |I| \sin \varphi} \tag{28}
\]

where the angle \( \varphi \) is the phase difference between the current phasor \( I_x \) and the corresponding voltage phasor \( V_{\phi n} \). In addition, \( |V_{\phi n}| \) is equal to the peak of source voltage \( (V_m) \) and the reactance \( X \) is equal to \( (L_f + L_a/2) \omega \). The amplitude of current phasor \( |I_x| \) depends on the active and reactive powers that are transferred between the MMC and the ac source, i.e.,

\[
|I_x| = \frac{S}{1.5 V_m}, \quad S = \frac{Q}{\sin \varphi} = \frac{P}{\cos \varphi} \tag{29}
\]

where \( P \) and \( Q \) represent the total active and reactive powers, respectively. Then, one can calculate the PQ chart of MMC (for a given \( L_f \)) by increasing the active power from zero to peak value and considering the following two constraints:

\[
\begin{align*}
|V'_{\phi}| & \leq \frac{V_d}{2} \\
|I_x| & \leq \frac{2I_{C_{nom}}}{3I_d}
\end{align*} \tag{30}
\]

where the first constraint is used to keep MMC in the linear modulation range, and the second constraint is applied to keep MMC IGBTs in the safe operating area. Based on given procedure, the PQ chart of MMC (studied in this article) is obtained and shown in Fig. 10 for three different cases.

From Fig. 10, it is seen that by insertion of ac reactors greater than 40 mH, the reactive power compensation capacity reduces in the capacitive mode. On the other side, by selecting a lower value of \( V_m \), the MMC can produce higher reactive power, but the capacity of active power transmission reduces. Finally, a rough cost comparison is made between the utilized HB-MMC, the presented hybrid dc breaker in [7], and the presented hybrid dc breaker in this article. At first, the required components of studied topologies are derived and listed in Table IV. In this article, the breakers are assumed to be unidirectional and the prices of components are determined approximately based on the price of one single IGBT (\( P_{IGBT} \)).
TABLE IV
NUMBER OF REQUIRED COMPONENTS AND PRICES FOR STUDIED SYSTEMS

<table>
<thead>
<tr>
<th>Component</th>
<th>Component price</th>
<th>HB-MMC</th>
<th>Breaker in [7]</th>
<th>Proposed Breaker</th>
</tr>
</thead>
<tbody>
<tr>
<td>IGBT 4.5 kV, 1.2 kA</td>
<td>P_{IGBT}</td>
<td>840</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>IGBT 4.5 kV, 2.2 kA</td>
<td>P_{IGBT}</td>
<td>840</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Thyristor 3.2 kV, 1 kA</td>
<td>0.15 P_{IGBT}</td>
<td>0</td>
<td>0</td>
<td>80</td>
</tr>
<tr>
<td>Diode 3.2 kV, 910 A</td>
<td>0.05 P_{IGBT}</td>
<td>0</td>
<td>0</td>
<td>80</td>
</tr>
<tr>
<td>Capacitor 7 mF, 3.3 kV</td>
<td>3 P_{IGBT}</td>
<td>420</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Reactor</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C702CB</td>
<td>48 P_{IGBT}</td>
<td>0</td>
<td>0</td>
<td>6</td>
</tr>
<tr>
<td>VS-SD1100C32L</td>
<td></td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>947C102K112DEHS</td>
<td></td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
</tbody>
</table>

Also, the cost of MOVs and resistors are not considered in this article.

In Table IV, the prices of reactors are estimated based on a given “price chart” in [30], which is suitable for high-voltage dry-type series reactors. Also, the current and inductance values are scaled based on the given formula in [29], i.e., \( C \propto I \sqrt{L} \), where \( C \) is the reactor cost, \( I \) is the coil nominal current, and \( L \) is its inductance. Based on Table IV, the prices of different elements are obtained and normalized with respect to the total price of HB-MMC and listed in Table V.

From Table V, it is concluded that the cost of extra ac reactors is about 46% of the hybrid dc breaker. Also, the total cost of new breaker is almost 12% of the designed HB-MMC.

### V. EXPERIMENTAL INVESTIGATION

In this section, the experimental results of the scaled down system for testing the new hybrid dc breaker are given. The photo of hardware prototype is shown in Fig. 11, and the system parameters are given in Table VI. In this prototype, each arm contains four half-bridge SMs and a combination of TMSF2833 DSP and SPARTAN-6 FPGA are employed for the control system. In addition, design parameters of the hybrid dc breaker are same as Table VI, except that \( I_f = 2I_d = 12 \) A, \( V_{\text{lcs, max}} \leq 0.05 \times V_d = 7.5 \) V, and \( I_{\text{arm, max}} \leq 14 \) A. Calculated design parameters are listed in Table VII.

The first experiment investigates the operating principle of a new hybrid dc breaker when the MMC system is working at the nominal condition and a short-circuit fault occurs at the dc-side. The key waveforms \( i_d, i_{\text{lcs}}, i_1, \) and \( V_{\text{lcs}} \) are obtained and demonstrated in Fig. 12.
As it is seen in Fig. 12, at \( t = t_1 \) the protection system is activated and the Thyristor \( T_{1i} \) is turned ON. Also, the MMC is programmed to synthesize zero voltages at all arms. Then, after 0.5 ms, the LCS is turned OFF and the turn-OFF command is sent to MD. At \( t = t_2 \) (or about 4 ms after the fault confirmation at \( t = t_2 \)), the LCS current becomes zero and the fault current is cleared. Finally, at \( t = t_3 \) (or 5 ms after the fault confirmation at \( t = t_2 \)), MMC IGBTs are turned OFF. It is evident that the LCS voltage remains lower than 7.5 V (\( v_{lcs} < 0.05 \times V_d \)) at the whole period and satisfies the design goal.

Fig. 13 demonstrates the MMC upper arms currents during the fault clearing period. Based on the demonstrated waveforms, the peak arm current in the fault clearing state is about 14 A and satisfies the design goal \( I_{arm,max} \leq 14 \text{ A} \).

To implement the presented hybrid dc breaker in a real MMC application, design considerations of high-voltage systems must be taken into account. For example, the proposed structure needs a Thyristor valve that is made of series-connected Thyristors. For the Thyristor valve not only the turn-on and turn-off snubbers are needed, but also extra passive snubbers are needed to prevent voltage imbalance among series devices. Also, the commutation time of fault current from the LCS to Thyristor valve is not negligible and it may take up to 250 \( \mu \text{s} \) [21]. The last point, but not the least: with the distributed control system in real MMCs, the communication delay must be taken into account and compensated by software techniques.

VI. CONCLUSION

In this article, a modified hybrid dc breaker was introduced to interrupt the dc fault current by the help of Hb-MMC. The proposed method replaces the semiconductor breaker and the MOV arrester with a Thyristor valve and an energy-absorbing capacitor. In contrast to conventional hybrid dc breakers that employ ultrafast mechanical disconnectors, this approach can employ slower mechanical disconnectors without any performance deterioration. In addition, the current in the hybrid dc breaker remains always lower than the trip level and the arms currents are kept lower than the specified limit. An analytical approach was introduced to design the hybrid dc breaker. Although the total semiconductor loss in the proposed method was 1.0% higher than the conventional approach but its simplicity and higher reliability (due to lower stress on the mechanical part and semiconductor breaker) compensated its weak point.

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