A Method to Control the Interphase Power Controller with Common DC Bus

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Abstract—Increasing number of interconnections at a power system network raises the short circuit current levels and may cause to replace part of protecting equipment. The interphase power controller (IPC) is capable to control the power flow and to limit the short circuit current. This paper presents a control method for the IPC with common DC bus which is an alternative to phase-shifting transformers. The model of a common DC bus IPC is developed in d-q frame and based on it a control system is proposed to regulate the active power flow. The utilized structure has more flexibility in controlling the power system compared to previously proposed IPCs which are based on static synchronous series compensator. An experimental setup based on cascaded H-bridge converters has also been implemented to verify the proposed control method. Both the simulation and experimental results confirm the ability of common DC bus IPC with the proposed control method in power flow control and short circuit current limitation.

1. INTRODUCTION

Interphase power controller (IPC) is one of the flexible AC transmission system (FACTS) devices that is used both as a fault current limiter and power flow controller for networks. The IPC is a series connected device that has two parallel inductive and capacitive branches and each of the branches is in series with a separate phase-shifted voltage source as can be seen in Figure 1. The main IPC design parameters are the values of inductor \((L)\), capacitor \((C)\), and the control parameters that determine the magnitude and phase angles of the injected voltages \(\vec{V}_{c1}\) and \(\vec{V}_{c2}\).

In short circuit mitigation applications, the impedances of the reactor and the capacitor at IPC structure are tuned at the fundamental frequency of network (50 or 60 Hz), so during short circuit time, the IPC operates like an infinite impedance [1]. Also in tuned IPC, each of terminals behaves as a voltage dependent current source [2].

IPC implementations are divided to four categories.

1.1. IPC Based on Passive Components

The first category consists of passive components such as reactor, capacitor, transformers and phase-shifting...
transformers (PST) [3]–[8]. In the structure of IPC240, a reactor and capacitor are in series with a separate phase-shifting voltage in each phase [3]. In IPC120, to improve the power factor of IPC240, a Y-y6 transformer has been used.

In [9], the installation of the first IPC to increase the capacity of power flow between New York Power Authority and VELCO systems at Plattsburgh substation is described. To increase the power flow, a reactor was paralleled with the existing PST, and this structure has been called "assisted phase-shifting transformers (APST)." The schematic of this structure has been presented in [10].

An algorithm has been proposed in [11] for designing and selecting the main components of IPCs such as necessary phase angles of PSTs and reactance values of inductor and capacitor. This algorithm has been utilized in the paper for sizing the IPC elements.

At some structures in this group, the transformer rated power has to be equal to the maximum power that is transferred through the transmission line. Moreover, additional passive components such as PSTs will add to the cost of this group.

1.2. IPC Based on Active Components

In the second category, the IPC based on active components has been proposed, in which low frequency switches like Thyristors have been used [12]–[16].

By replacing PSTs in IPC structure with parallel or series voltage source converters, new categories of IPCs have been proposed in [17], [18]. Voltage source converters based on power electronic semiconductors, improve the dynamic behavior of IPC and its flexibility in power management. Also, the total harmonic distortion (THD) of this device is lower than Thyristor based IPC.

1.3. IPC Based on Parallel Converter

In the third category of IPC, the DC link voltage of each voltage source is controlled by a parallel converter [19]–[21]. For independent control of active and reactive power in the transmission line, a unified power flow controller (UPFC) has been employed at internal structure of IPC [20]. Although this structure has the capability of superior power control, it suffers from the increased cost.

In order to synthesize the required voltage levels, cascaded H-bridge based IPC (CHB-IPC) has been presented in [19], where the DC links are charged by parallel rectifiers. Implementation of this topology is also expensive because of using separate rectifiers.

1.4. IPC Based on Series Converter

In the fourth category, the DC link voltage is controlled by series converter. The static synchronous series compensator (SSSC) only exchanges the reactive power and may be considered instead of PST [23]. In [17], the mathematical modeling of IPC based on the SSSC has been reviewed and the ability of short circuit current reduction and better power flow management at power network has been verified by simulation study. This topology can be realized with lower cost compared with the UPFC [20], [21] or CHB based IPC in [19]. But the control of SSSC based IPC is more complex than other categories because of limitation in injecting active power into IPC branches and needs to sophisticated control methods. The IPC with common DC bus needs only one DC bus compared to two separate DC buses that are required in the SSSC based IPC, and has the ability of transferring active power between branches [21].

In this paper, common DC bus IPC structure, which has less converter than third category, is selected for study. The model of this structure is derived in d-q frame. Then, based on simplified equations, a control system is proposed to control the active power flow at steady-state or in quasi-state operation. To verify the performance of the new control approach, a part of real 230 kV power system network is selected as a case study for simulation part. Moreover, to confirm the simulation results, a laboratory prototype of this structure with two 7-level CHB converters is also implemented. The advantages of this structure and the control system can be listed as follows: (1) The selected structure has less number of components compared to third category. (2) The number of DC links is lower than other structures. (3) The power can be transferred between branches. (4) The control system is simpler than non-linear control strategies, which have been used in previous articles. (5) The control system does not need to sense the current of inductive and capacitive branches compared to SSSC based IPC.
2. IPC WITH COMMON DC LINK

2.1. Structure

The single-line diagram of IPC with common DC link is shown in Figure 2, which contains two voltage source converters with a common DC link. The utilized parameters in Figure 2 are defined in d-q frame and are listed in Table 1.

2.2. System Modeling

According to Figure 2, the following equations are derived for the AC and DC sides of the converters [22]:

\[
\begin{align*}
\left( L_x \frac{d i_d}{dt} - L_x \omega i_q \right) + R_x i_d + \left( L_x \frac{d i_q}{dt} - L_x \omega i_d \right) \\
= V_{dS} - V_{dR} - u_{d1} V_{Cdc}
\end{align*}
\]

(1)

\[
\begin{align*}
\left( L_x \frac{d i_d}{dt} - L_x \omega i_q \right) + R_x i_d + \left( L_x \frac{d i_q}{dt} - L_x \omega i_d \right) \\
= V_{qS} - V_{qR} - u_{q1} V_{Cdc}
\end{align*}
\]

(2)

\[
\begin{align*}
\frac{d v_{dL}}{dt} + R_x i_d + \frac{C}{L_x} i_q \\
= V_{dS} - V_{dR} - u_{d2} V_{Cdc}
\end{align*}
\]

(3)

\[
\begin{align*}
\frac{d v_{qL}}{dt} + R_x i_d + \frac{C}{L_x} i_q \\
= V_{qS} - V_{qR} - u_{q2} V_{Cdc}
\end{align*}
\]

(4)

The power balance of the AC and DC sides in each converter and the relationship between the voltage and the current of DC link capacitor lead to the following equation:

\[
\begin{align*}
u_{d1} i_{dL} V_{Cdc} + u_{q1} i_{qL} V_{Cdc} + u_{d2} (i_d - i_{dL}) V_{Cdc} \\
+ u_{q2} (i_q - i_{qL}) V_{Cdc} = C_{dc} \frac{d V_{Cdc}}{dt} V_{Cdc} + (G_1 + G_2) V_{Cdc}^2
\end{align*}
\]

(5)

by dividing each side of (7) by \( V_{Cdc} \), the following equation is derived:

\[
\begin{align*}
u_{d1} i_{dL} + u_{q1} i_{qL} + u_{d2} (i_d - i_{dL}) + u_{q2} (i_q - i_{qL}) \\
= C_{dc} \frac{d V_{Cdc}}{dt} + (G_1 + G_2) V_{Cdc}
\end{align*}
\]

(8)

The aforementioned state equations can be presented as follows for multiple input multiple output (MIMO) non-linear systems:

\[
\dot{x} = f(x) + \sum_{i=1}^{4} g_i \cdot u_i
\]

(9)

where the state variables and control inputs are defined as follows:

\[
x = \begin{bmatrix} i_{d1}, i_{d2}, i_q, i_{qL}, V_{Cdc}, V_{dC}, V_{qC} \end{bmatrix}^T
\]

(10)

\[
u = \begin{bmatrix} u_{d1}, u_{q1}, u_{d2}, u_{q2} \end{bmatrix}^T
\]

(11)

\[
f(x) = \begin{bmatrix}
\frac{L_x i_{dL} + L_x i_{qL}}{L_x}
-rac{V_{dS} - V_{dR} - u_{d1} V_{Cdc}}{L_x}
-rac{V_{qS} - V_{qR} - u_{q1} V_{Cdc}}{L_x}
-rac{L_x i_{d2} + L_x i_{q2}}{L_x}
-rac{(G_1 + G_2) V_{Cdc}}{L_x}
-rac{i_q - i_{qL} + C_{dc} V_{Cdc}}{L_x}
-rac{i_d - i_{dL} + C_{dc} V_{Cdc}}{L_x}
\end{bmatrix}
\]

(12)
3. CONTROL STRATEGY

3.1. Deriving Steady-State System Equations

The output variables of control system are the active powers and the DC link voltage. The transmitted active and reactive powers are related to line current and voltage of receiving terminal as follows:

\[ p = 1.5(V_{dRi_d} + V_{qRi_q}) \quad (14) \]
\[ q = 1.5(V_{qRi_d} - V_{dRi_q}) \quad (15) \]

In order to find a simple method for controlling the line power flow, this paper considers the system Eq. (9) at steady-state. In steady-state and in d-q frame, the state variables become DC values, i.e., \( \dot{x} = 0 \); therefore,

\[ i_d - i_{dL} + C\omega V_{qC} = 0 \Rightarrow V_{qC} = \frac{(i_{dL} - i_d)}{C\omega} \quad (16) \]
\[ -i_q + i_{qL} + C\omega V_{dC} = 0 \Rightarrow V_{dC} = \frac{(i_q - i_{qL})}{C\omega} \quad (17) \]

by substituting (17) into (9), the following relation is achieved.

\[ \frac{i_q}{C\omega} + \left( L\omega - \frac{1}{C\omega} \right) i_{qL} + (u_{dL} - u_{d1}) V_{Cdc} = 0 \quad (18) \]

With neglecting the leakage impedance of isolating transformer and assuming that the reactance of inductive and capacitive branches are equal, i.e., \( X_a = L\omega = \frac{1}{C\omega} \), one can obtain \( i_q \) from (18).

\[ i_q = \frac{(u_{d1} - u_{dL}) V_{Cdc}}{X_a} \quad (19) \]

In addition, substituting (16) into (9) leads to:

\[ \frac{i_d}{C\omega} - u_{q2} V_{Cdc} + u_{q1} V_{Cdc} + \left( L\omega - \frac{1}{C\omega} \right) i_{dL} = 0 \quad (20) \]

In similar way \( i_d \) can be derived from (20) as follows:

\[ i_d = \frac{(u_{q2} - u_{q1}) V_{Cdc}}{X_a} \quad (21) \]

\[ g(x) = \begin{bmatrix} 0 & 0 & -\frac{-V_{Cdc}}{L} & 0 \\ -\frac{-V_{Cdc}}{L} & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{-V_{Cdc}}{L} \\ \frac{i_{dL}}{C\omega} & \frac{i_{qL}}{C\omega} & \frac{-i_{dL}}{C\omega} & \frac{-i_{qL}}{C\omega} \\ 0 & 0 & 0 & 0 \end{bmatrix} \quad (13) \]

\[ \begin{bmatrix} -1 \omega & -\frac{-V_{Cdc}}{L} \\ -\frac{-V_{Cdc}}{L} & 0 \\ 0 & -\frac{-V_{Cdc}}{L} \\ \frac{i_{dL}}{C\omega} & \frac{i_{qL}}{C\omega} \\ 0 & 0 & 0 & 0 \end{bmatrix} \]

3.2. Control of Active Power Flow

Figure 3 shows the phasor diagram of IPC with common DC link. \( V_{c1} \) and \( V_{c2} \) represent the injected voltages in inductive and capacitive branches, respectively.

As can be seen, \( \vec{V}_a \) is along with d axis. \( \vec{V}_{c1} \) and \( \vec{V}_{c2} \) can be decomposed into \( (V_{d1}, V_{q1}) \), and \( (V_{d2}, V_{q2}) \), respectively, where \( V_{d1} \) and \( V_{d2} \) are in phase with \( \vec{V}_d \). Since the phase difference between \( \vec{V}_a \) and \( \vec{V}_c \) is usually small, \( |V_{dc}| \) is much bigger than \( |V_{qR}| \). Therefore, according to (22), \( u_{q1} \) and \( u_{q2} \) can be selected to control the active power \( P \). Moreover, \( u_{d1} (u_{d1} = V_{d1}/V_{Cdc}) \) and \( u_{d2} (u_{d2} = V_{d2}/V_{Cdc}) \) can be used to control the DC bus voltage, because according to Figure 3, these voltage components have more effect on absorbing power from the IPC branches. In (22), the term \( (u_{d1} - u_{d2}) V_{qR} \) is much smaller than the first term and it can be neglected. Using this assumption, Eq. (22) is simplified as follows:

\[ p \approx \frac{3}{2} V_{dR} \frac{(u_{q2} - u_{q1}) V_{Cdc}}{X_a} \quad (24) \]

It is seen that the active power can be controlled using \( u_{q1} (u_{q1} = V_{q1}/V_{Cdc}) \) and \( u_{q2} (u_{q2} = V_{q2}/V_{Cdc}) \). According to (24), in the case that two controlling parameters have opposite signs, the flow of active power is increased while in the case that two variables have the same signs, the power flow is reduced at the transmission line. In (23), due to the use of \( u_{q1} \) and \( u_{q2} \) for control of active power, independent control of both active and reactive power is not possible.
Based on (24), a control system is proposed which only controls the active power flow. Two different cases are considered, which are related to positive and negative power flows. For positive power flow, \((u_{q2} - u_{q1})\) should be positive and for negative power flow, \((u_{q2} - u_{q1})\) should be negative. Moreover, to achieve the almost equal loading for two VSCs, it is assumed that \(|u_{q2}| = |u_{q1}|\) in both cases.

In the IPC, the DC bus capacitor voltage can be regulated by the inductive or capacitive branch currents. It is more convenient to choose the branch in which its current sign does not change over the whole range of power flow. Figure 4 shows the phasor diagrams of the IPC voltages and currents, where Figures 4(a) and 4(b) hold for the positive power flow, and Figures 4(c) and 4(d) correspond to negative power flow. Based on Figures 4(a) and 4(b), the sign of current in capacitive branch under positive power flow will change as the power flow increases. This fact is realized from the phase change of \(\vec{V}_2\) respect to \(\vec{V}_m\). Therefore, under positive power flow, \(u_{dl}\) (related to inductive branch) is preferred for regulation of DC bus voltage and \(u_{dl}\) (related to capacitive branch) is preferred in case of negative power flow.

Based on the above discussion, the demonstrated control block diagram in Figure 5 is proposed for active power control.

In the proposed control system, there is no need to sense the current of branches and the voltage of capacitor in capacitive branch for control purposes compared to SSSC based IPC. The current sensors, however, may be employed for protection purposes. Also, the other advantage of the proposed controller is the simplicity compared to other non-linear control strategies [22]. For example, a high number of state variable sensors and a power full processor are necessary in non-linear control system. In addition, for the sake of achieving linearity, a feedback linearizing controller may generate unnecessarily large control effort to cancel beneficial non-linearities [24].

4. NETWORK MODELLING AND THE STRUCTURE OF MULTILEVEL VOLTAGE SOURCE CONVERTERS IN THE IPC

The performance of the IPC is evaluated in a section of 230 kV network as shown in Figure 6. Here, the IPC is placed on the bus 3400 between the buses “3450” and “3430.” The parameters of the network are given in Table 2. More details about this network can be found in [11], [18], [19].

In order to work at high voltages and to achieve a low THD output voltage, the CHB structure is employed in the proposed topology. The CHB converter is extremely modular and needs the least number of components to produce the same number of voltage levels compared to the other topologies. The main

FIGURE 4. Phasor diagrams of IPC voltages and currents at different levels and directions of power flow. (a) At lower positive power flow. (b) At higher positive power flow. (c) At lower negative power flow. (d) At higher negative power flow.
drawback of this topology is necessity of isolated DC sources. Hence, to employ this topology in back-to-back connection, isolating transformers have to be used in the structure of IPC. In this paper, two 7-level CHB converters with common DC links are used. This structure is shown in Figure 7(a). As it can be seen, each voltage component of inverters in Figure 2 divided into three parts \( V_{d1} \rightarrow V_{d11}, V_{d12}, V_{d13}; V_{q1} \rightarrow V_{q11}, V_{q12}, V_{q13}; V_{d2} \rightarrow V_{d21}, V_{d22}, V_{d23}; V_{q2} \rightarrow V_{q21}, V_{q22}, V_{q23} \) in Figure 7(a). The control block diagram for this structure is shown in Figure 7(b). As it can be seen each DC link voltage is separately regulated by a controller, also the reference value for each DC link can have different values. In this work, phase shifted pulse width modulation is used to generate multilevel voltage waveforms.

5. SIMULATION RESULTS

To show the performance of the common DC bus IPC, part of 230 kV transmission network is selected to be investigated in Matlab/Simulink environment. The utilized simulation parameters are shown in Table 3.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal base power</td>
<td>( S_{\text{base}} )</td>
<td>100 MVA</td>
</tr>
<tr>
<td>Line voltage</td>
<td>( V_{\text{LL}} )</td>
<td>230 kV</td>
</tr>
<tr>
<td>Number of H-Bridge modules</td>
<td>( N )</td>
<td>3</td>
</tr>
<tr>
<td>Transformer ratio</td>
<td>( n_1 )</td>
<td>1</td>
</tr>
<tr>
<td>( n_2 )</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>DC link voltage of the CHB converter</td>
<td>( V_{\text{DC}} )</td>
<td>18 kV</td>
</tr>
<tr>
<td>Network frequency</td>
<td>( f )</td>
<td>50 Hz</td>
</tr>
<tr>
<td>Switching frequency of converters</td>
<td>( f_{\text{sw}} )</td>
<td>750 Hz</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( Z_1 )</td>
<td>0.0001 + j0.0017 p.u.</td>
</tr>
<tr>
<td>( Z_2 )</td>
<td>0.0002 + j0.0028 p.u.</td>
</tr>
<tr>
<td>( Z_r )</td>
<td>0.00118 + j0.00595 p.u.</td>
</tr>
<tr>
<td>( Z_s )</td>
<td>0.00165 + j0.01315 p.u.</td>
</tr>
<tr>
<td>( X_a )</td>
<td>0.17 p.u.</td>
</tr>
<tr>
<td>( \angle V_1 - \angle V_2 )</td>
<td>4.4°</td>
</tr>
</tbody>
</table>

**TABLE 2.** Network parameters.

**TABLE 3.** Simulation parameters used for investigation.
Figure 8(a) shows the active power reference and the transmitted power flow values. As it can be seen, the active power is able to follow the reference value in all conditions.

Figure 8(c) shows the generated 7-level voltage by the converters at $P = 320$ MW. These voltages are out of phase, because $u_{q1}$ and $u_{q2}$ have opposite signs. The branch currents and the DC link voltage are shown in Figures 8(b) and 8(d) respectively. Based on (8), the DC link voltage is dependent on $u_{q1}$ and $u_{q2}$, so when the active power reference changes, the value of $u_{q1}$ and $u_{q2}$ is set by the power controller and it may change the DC bus voltage, but the DC link voltage controller set the DC values to the desired reference.

6. EXPERIMENTAL RESULTS

To show the validity of common DC bus IPC in practice, a single phase implementation of the power network (based on section IV) is realized. In this laboratory prototype, two 7-level CHB converters which have common DC buses with isolating transformers are used. Moreover, the proposed control algorithm is implemented in a CORTEX M4 ARM

![Figure 9](image)

**Figure 9.** The test bench of IPC hardware.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal base power (single phase)</td>
<td>$S_{base}$</td>
<td>600 VA</td>
</tr>
<tr>
<td>Phase voltage</td>
<td>$V_{ph}$</td>
<td>311 V</td>
</tr>
<tr>
<td>Number of H-Bridge modules</td>
<td>$N$</td>
<td>3</td>
</tr>
<tr>
<td>Power Switch</td>
<td>$S$</td>
<td>IRF540N</td>
</tr>
<tr>
<td>Nominal power of transformer</td>
<td>$S_T$</td>
<td>100 VA</td>
</tr>
<tr>
<td>Transformer ratio</td>
<td>$n_2$</td>
<td>1</td>
</tr>
<tr>
<td>DC link voltage</td>
<td>$V_{dc}$</td>
<td>90 V</td>
</tr>
<tr>
<td>DC link voltage of the CHB converter</td>
<td>$V_{dc}$</td>
<td>30 V</td>
</tr>
<tr>
<td>Network frequency</td>
<td>$f$</td>
<td>50 Hz</td>
</tr>
<tr>
<td>Switching frequency of converters</td>
<td>$f_{sw}$</td>
<td>750 Hz</td>
</tr>
<tr>
<td>The IPC inductor</td>
<td>$L$</td>
<td>122 mH</td>
</tr>
<tr>
<td>The IPC capacitance</td>
<td>$C$</td>
<td>83 μF</td>
</tr>
<tr>
<td>DC Capacitance</td>
<td>$C_{dc}$</td>
<td>6 mF</td>
</tr>
</tbody>
</table>

**Table 4.** The parameters for the hardware prototype.
FIGURE 10. Experimental evaluation of active power control. Reference is changed from (a) 200 to 400 (b) 600 to 400 (c) 200 to −200 (d) −400 to −600.

FIGURE 11. Experimental investigation of active power control. (a) Voltage and current of line when $P = −600$ W. (b) Injected voltages at $P = −600$ W. (c) Inductive and capacitive branch currents at $P = −600$ W. (d) DC link voltages.
FIGURE 12. Investigation of fault scenario. (a) Fault location in transmission line. (b) Voltage and current without IPC during fault time. (c) Voltage and current with IPC during fault time.

6.1. Scenario 1: Active Power Control

In this test, active power reference is changed and the recorded values for active power are demonstrated in Figure 10. According to the results, control system can follow the power flow reference in less than 1 sec, in different test scenarios. Furthermore, corresponding voltage and current waveforms when the active power is $-600\ W$ is shown in Figure 11. The line voltage and current are shown in Figure 11(a). The injected voltages, the inductive and capacitive branch currents and DC link voltages are shown in Figures 11(b), 11(c), and 11(d), respectively.

6.2. Scenario 2: Short Circuit Current Mitigation

In this section, a short circuit test is performed to show the ability of IPC in fault current limitation. The fault location in transmission line is shown in Figure 12(a). The short circuit time period is about 1.5 cycle and fault resistance is equal to the resistance of Triac which is used for fault generation. 5 ms after the fault, the CHB converters are bypassed by the Triacs $Q_1$ and $Q_2$ and IPC acts as a fault current limiter. Moreover, in the test period, the phase voltage is set to 100 V. Figure 12(b) shows the line current without presence of IPC. As can be seen, the peak of fault current is about 70 A. However, as it can be seen in Figure 12(c), the short circuit current is limited to 7 A with the IPC. The branch currents and DC link voltages are also shown in Figure 12(c).

7. CONCLUSIONS

In this work, based on IPC equations in d-q frame, a control system was extracted. The proposed control system has some advantages such as simplicity compared to other non-linear control strategies and no necessity to sense the current of branches compared to previous structures. To verify the performance of the proposed controlling system, part of a sample 230 kV network was selected and simulated in Matlab/Simulink environment. To confirm the simulation results, a laboratory prototype of IPC based on CHB converters was built and tested. The experimental results of the prototype confirm the effectiveness of the IPC in power flow control. The short circuit current test on the proposed IPC proved the ability of IPC as a short circuit current limiter.

REFERENCES


**BIOGRAPHIES**

Mohammad Najjar received his B.S. degree in Electrical Engineering from the Islamic Azad University of Kazeroon, Fars, Iran, in 2010; and his M.S. degree in Power Electronics and Electrical Machines from the University of Tehran, Tehran, Iran, in 2014. His current research interests include multilevel converters, modeling and control of power electronic converters, FACTS devices and power quality issues.

Shahrokh Farhangi received his B.S., M.S. and Ph.D. degrees in Electrical Engineering (Hons.) from the University of Tehran, Tehran, Iran. He is presently working as a Professor in the School of Electrical and Computer Engineering, University of Tehran. He has published more than 100 papers in journals and conference proceedings, and was selected as a Distinguished Engineer in Electrical Engineering by the Iran Academy of Sciences in 2008. He has managed several research and industrial projects, some of which have won national and international awards. He was the recipient of a Paper Award in 2011, and an American Geophysical Union
Outstanding Student Paper Award in fall 2005. His current research interests include the design and modeling of power-electronic converters, drives, photovoltaics, and renewable energy systems.

**Hossein Iman-Eini** received his B.S. and M.S. from University of Tehran, Tehran, Iran, in 2001 and 2003, respectively, and his Ph.D. from both University of Tehran and Grenoble Institute of Technology, France, in 2009, all in electrical engineering. He is currently an associate professor in the School of Electrical and Computer Engineering, University of Tehran. His current research interests include the modeling and control of power converters, multi-level converters, and renewable energy systems.