Integration of highly-strained SiGe materials in 14 nm and beyond nodes FinFET technology

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Abstract

SiGe has been widely used as stressors in source/drain (S/D) regions of Metal–Oxide–Semiconductor Field Effect Transistor (MOSFET) to enhance the channel mobility. In this study, selectively grown Si$_1$Ge$_x$ (0.33 $\leq x \leq 0.35$) with boron concentration of 1 $\times$ 10$^{20}$ cm$^{-3}$ was used to elevate the S/D regions on bulk FinFETs in 14 nm technology node. The epitaxial quality of SiGe layers, SiGe profile and the strain amount of the SiGe layers were investigated. In order to in-situ clean the Si-fins before SiGe epitaxy, a series of prebaking experiments at temperature ranging from 740 to 825 $^\circ$C were performed. The results showed that the thermal budget needs to be limited to 780–800 $^\circ$C in order to avoid any damage to the shape of Si-fins but to remove the native oxide which is essential for high epitaxial quality. In this study, a kinetic gas model was also applied to predict the SiGe growth profile on Si-fins with trapezoidal shape. The input parameters for the model include growth temperature, partial pressures of reactant gases and the chip layout. By knowing the epitaxial profile, the strain to the Si-fins exerted by SiGe layers can be calculated. This is important in understanding the carrier transport in the FinFETs. The other benefit of the modeling is that it provides a cost-effective alternative for epitaxy process development as the SiGe profile can be readily predicted for any chip layout in advance.

1. Introduction

The transition from planar transistors to 3D FinFETs is an important technological step for Complementary Metal–Oxide–Semiconductor (CMOS) technology since the performance of the transistors can remarkably be improved [3,2]. For the 3D transistors, strain engineering is crucial to enhance the channel mobility. This may be achieved, for instance, when SiGe material with high Ge content is selectively deposited on source/drain areas [4,12,17,18]. In general, a FinFET is designed by parameters such as the height and width of the fin, doping level and geometry of sidewalls [13]. The last parameter is controlled by an anisotropic over-etch when trapezoid or triangular fins are processed.

The fin geometry has an important role in SiGe strain amount. As an example, the quality of growth can be affected more on the sidewalls compared to the central part of fins [1].

The deposition of SiGe on Si-fins is a very sensitive process and the layer quality may degrade due to any undesired residual species (after the etch step) or native oxide. In this case, the ex- and in-situ cleaning are important steps prior to the epitaxy.

One of the major concerns about selective epitaxy growth is that the SiGe layer profile depends on the pattern layout (shape, size and density of the openings) as well as wafer architecture (oxide or nitride). This dependency originates from lateral diffusion characteristics of gas molecules above the wafer or on the oxide surface [6,10,15,5,9,8]. Different methods have been reported to make more uniform SiGe profiles but none of these methods could effectively eliminate the pattern dependency of the growth. Therefore, a theoretical calculation to determine the SiGe profile for different mask designs can be useful for chip manufacturers.

This article presents the integration of selective epitaxy of highly strained SiGe layers in 14 nm node FinFETs. Furthermore, a kinetic model is presented to estimate the SiGe layer profile on Si-fins with trapezoidal shape. The model takes into account the gas kinetics and diffusion of the formed/dissociated molecules on the fins for any advanced chip design.

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2. Experimental details

The experiments in this work have been performed on patterned 8-in. wafers in the process line of 14 nm technology node for FinFETs. Sidewall transfer lithography (STL) was utilized to pattern the Si-fins with 15 nm top width and 110 nm height. In this process, Si₃N₄/SiO₂ spacers of 20 nm width were applied as hard mask. An anisotropic dry etch of the bulk was then performed to form trapezoid-shape Si-fins. The remaining spacers were then stripped in hot H₃PO₄ and dilute HF solution in sequence. A sacrificial oxidation in a rapid thermal processing (RTP) chamber were carried out in order to repair the plasma damage to fins caused by the dry etching as well as to round the Si-fin corners. Afterwards, a 2000 Å thick high-aspect-ratio process (HARP) oxide film was deposited as shallow trench isolation (STI) oxide and chemical mechanical polishing (CMP) was used to planarize the topography. By means of the combination of dry etch and wet etch in diluted HF solution, the STI oxide was recessed to expose the fins. A dummy α-Si gate was patterned by electron beam lithography (EBL) crossing over the fins followed by spacer formation at both sides. All samples were cleaned using a standard cleaning procedure prior to epitaxy (SPM followed by APM with DHF at last). The load-locks were pumped down rapidly in order to avoid any surface contamination on the wafers.

The SiGe layers were grown on Si-fins at 650 °C in an RPCVD reactor. In-situ cleaning was performed by annealing in the range of 740–825 °C for 3–7 min. Dichlorosilane (SiH₂Cl₂), 10% germane (GeH₄) in H₂ and 1% diborane (B₂H₆) in H₂ were used as Si, Ge and B precursors, respectively. HCl was utilized as the Si etchant to obtain selectivity during the epitaxy. The whole FinFET areas were covered by SiO₂ and planarized by a CMP step. This oxide is related to thermal mismatch between Si and SiO₂. More Ge atoms are expected on the oxide surface during epitaxy. In Fig. 1(e), the oxide is expected to be present at the surface in form of islands with small sizes. These islands have arisen in processing fins with regular shapes and controlled sidewall edges. To induce high strain amount in the channel region, the pre-baking of Si-fins is an important step prior to the epitaxy to remove any native oxide or residual impurities on the Si surface. However, Si-fin is a delicate part of a FinFET structure where its shape can be damaged by an annealing treatment. The previous studies have demonstrated that the geometry of Si-fin as well as body doping level will affect the threshold voltage and carrier profile of FinFET. For example, more inclination angle of sidewalls and doping level of ~10¹⁷ cm⁻³ are desired to increase the threshold voltage [13]. Both these parameters are dependent on the thermal budget of the process.

Fig. 1(a–f) shows HRSEM cross-section micrographs of Si-fins. The first micrograph shows a processed Si-fin without any epitaxial layer as reference sample (Fig. 1(a)). The shape of the Si-fins in this sample is intact without any deformation. Fig. 1(b–e) shows epitaxially deposited SiGe layers on top of Si-fins. These samples are baked at temperatures 740–825 °C prior to epitaxy (in-situ cleaning step). However, the original shape of the Si-fin is affected after prebaking at 825 °C (Fig. 1(b)). This figure shows a serious Si loss and as a result, the height of the fin has shrunk. Although the surface of Si-fins is damaged but SiGe layer could still be grown with reasonable quality.

The irregularity of Si-fins’ shape at high temperature annealing is related to thermal mismatch between Si and SiO₂. Since the expansion coefficient of SiO₂ layer is lower than Si (2.6 × 10⁻⁶ and 5 × 10⁻⁷ °C⁻¹, respectively), a non-uniform expansion during an annealing treatment occurs. The effect is so strong at 825 °C that results in breaking the Si-fins. A remedy to this problem is lowering the thermal budget. Samples with 800 and 780 °C prebaking in Fig. 1(c) and (d), respectively, have high quality Si-fins and SiGe layers.

In general, a condition for a successful SiGe growth is that the layer coverage over the Si-fin should be symmetric. The symmetry is important since it determines the uniformity of strain over Si-fins. Among the micrographs in Fig. 1, the symmetric feature of SiGe layer decreases by lowering the prebaking temperature to 760 °C (Fig. 1(c–e)). This problem becomes even more severe at lower annealing temperatures where the SiGe growth becomes entirely non-uniform over Si-fin surface for samples treated at 740 °C (Fig. 1(f)). The deformation of the SiGe layer on the Si-fin in Fig. 1(e) and (f) is a result of the residual native oxide on the Si-fin surface. Therefore, a thermal budget of 780–800 °C is proposed for 14 nm node FinFET technology.

In this study, more detailed investigation was performed to detect defects and to figure out the Ge content both in vertical and horizontal direction in the epi-layers by using TEM in combination with EDS techniques. Fig. 2(a) and (b) shows the TEM image and EDS spectra for the 800 °C prebaked sample in Fig. 1(c). In some cases, the SiGe contained stacking faults at the border between (1 1 1) and (0 0 1) facet planes. In EDS analysis, Ge, Si and O signals have been traced versus beam position in nm-scale. The position of the analyzed fin is in the middle of the chip in a region with exposed Si area of 2.5% of the whole area. The Ge content within SiGe layer is uniformly distributed with a symmetric feature. An estimation of 35% for Ge content is obtained when contribution of all signals are taken into consideration.

A similar TEM and EDS analysis were performed for 760 °C prebaked sample (in Fig. 1(e)) and the results have been demonstrated in Fig. 3. A careful observation of the Ge and Si spectrum in Fig. 3(a) shows a slight enhancement of Ge content close to the Si-fin surface (during initial moments of epitaxy). Similar observation of slightly higher Ge content at two Si-fin sides can be scrutinized in Fig. 3(b). This behaviour can be explained by the presence of oxide residuals on Si (too low annealing temperature) and the selectivity behaviour during SiGe growth. In selective epitaxy, HCl ensures the selectivity mode on the oxide surface. As the etch rate of Si by HCl is higher than that of Ge, more Ge atoms are expected on the oxide surface during epitaxy. In Fig. 1(e), the oxide is expected to be present at the surface in form of islands with small sizes. These islands
do not affect the epitaxial quality severely but they may have influence on the Ge content.

In the above EDS analysis, ~20% of the oxygen signal represents a background level. For the following calculations, the oxygen and Si contents are corrected by reducing this ~20% value from the oxygen signal and adding it to the Si signal over the whole measurement range. The amount of this ~20% correction offset is obtained by considering the Si and oxygen signals over SiO₂ surface, as a reference (e.g. position 0~20 nm in Figs. 2(b) and 3(b)), where the atomic percentage of oxygen and Si in SiO₂ is known to be ~60% and ~40%, respectively. By applying the above correction, the amount of oxygen inside the SiGe/Si fins will be negligible.

In order to ensure the absence of oxygen in the fins, both Si and oxygen signals have been traced separately, as shown in Fig. 4. Si is detected inside the SiGe/Si fin and oxide layer (Fig. 4(a)). No oxygen is observed in the SiGe/Si fin. It is only present in the SiO₂ and in the thin native oxide on top of the SiGe (Fig. 4(b)).

The above analysis shows the Ge profile over Si-fins but for the device application, the strain is the main point of focus. The measurement of strain in SiGe layers over fins with a few nanometres size is not easy. In order to solve the problem, rocking curves were taken at (113), instead of (004), and afterwards were compared with (004) RCs. Fig. 5 shows these RCs from the sample in Fig. 1(c) which contains intrinsic SiGe layers with high epitaxial quality. The (004) scan illustrates a peak with very low intensity.
whereas (113) RCs have peaks with sufficient intensity for strain measurement.

For these X-ray measurements, the spot size of XRD was $10 \times 10 \text{ mm}^2$ in direct beam position. The incident beam angle for (113) reflection is as low as $2.6^\circ$ compared to $34.1^\circ$ for (004). In addition, a typical scan of $2^\circ$ in (113) reflection makes a grazing angle where many chips can be covered by X-ray beam and contribute to XRD signal. As a result, the SiGe peak is intense enough at (113) reflection and can be analyzed to estimate the strain amount. However, this peak is broadened which is a sign of strain distribution of SiGe layers. This is due to either the strain relaxation over different facet planes or variation of Ge content over the regions of the chip as a result of pattern dependency. In other words, the SiGe profile for fins may vary because of variation of layout in chips. The effect of pattern dependency has been discussed and modeled in the next section.

4. Calculation of SiGe profile over Si-fins

A theoretical model to describe the selective epitaxy of SiGe for 22 nm planar CMOS has been recently published in Ref. [3]. This model has been modified for the SiGe growth for 3D FinFETs. The modifications have considered the SiGe growth on a Si-fin surface containing a central part, (001) plane and (111) planes at the sides (for a fin with a trapezoid shape). The number of available dangling bonds and activation energies have to be modified for the growth of each of the different facet planes. Furthermore, an interaction term ($R^{IP}$) has been introduced in the model which takes into account the diffusion of the atoms from the (111) planes towards the central plane during 3D epitaxy.

In selective epitaxy, the growth is a result of etch and epitaxy at the same time where the latter process is dominant. So far, the strain in CMOS structures (from 90 nm down to 14 nm technology nodes) is induced by deposition of SiGe layers. In 14 nm node design, SiGe layers are grown on Si-fins to raise the source/drain areas. The source/drain on a Si-fin is defined after oxide is deposited and processed as a dummy gate prior to the epitaxy step.

The growth rate of SiGe on a Si-fin is a result of a series of contributions both in vertical and lateral directions as illustrated in Fig. 6. The impinging molecules (Si and Ge) perform deposition, while, at the same time, the Cl atoms etch away the absorbed atoms on the exposed Si areas and on the oxide surface. During the selective growth of SiGe, facet planes form both on the top and the bottom of the fins (Wulff shapes).

The main equation for the SiGe growth on a Si-fin structure can be written as following:

$$R_{Total} = R^V_{Si} + R^{LG}_{Si} + R^{SO}_{Si} + R^{CO}_{Si} + R^V_{Ge} + R^{LG}_{Ge} + R^{SO}_{Ge} + R^{CO}_{Ge} + R^{IP}_{Si} + R^{IP}_{Ge} + R^{IP}_{Cl}$$

Fig. 4. EDS analysis for a SiGe/Si-fin. (a) Si and (b) oxygen signals are measured independently.

Fig. 5. XRD rocking curves measured at (004) and (113) reflections (blue- and red-colored scan, respectively) from arrays of Si-fins over a test chip. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

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where \( R^p \) and \( R^{LC} \) are the contribution of gas molecules in vertical and lateral direction, while \( R^C \) and \( R^{CO} \) are for the reactant molecules (indexed with Si, Ge and HCl) moving on the oxide surface within or surrounding a chip, respectively. \( R^{CG} \) varies over regions where more oxide is available e.g. between two neighboring chips. \( R^P \) is the part of the Eq. (1) which represents the diffusion of atoms from the edges towards (001) plane in the centre of fins. The term \( R^P \) is one of the most important terms in Eq. (1) for the 3D growth of SiGe on Si fins which makes the equation different compared to our previous report for 2D growth.

The diffusion of adatoms over a Si-fin with facet planes is an important parameter which controls the kinetics of molecules. In this work, the diffusion theory for atoms over (001) and (111) surfaces has been applied [11,17]. According to this theory, the atoms on inclined planes have a longer diffusion length compared to (001) plane. Therefore, a flow of atoms from inclined planes at the sides is established towards the (001) plane in central part of Si-fins.

In this study, the growth temperatures for SiGe layers were in range of 600–650 °C. A diffusion length of ~200 and 300 nm is estimated for Si and Ge atoms, respectively. This means that both Si and Ge atoms will have the opportunity to migrate over the entire 14 nm Si-fins (on top and bottom facet planes) making a uniform SiGe profile. Thus, the contribution of \( R^P \) for Si-fins with such small size is negligible. In fact, this conclusion was expected since the experimental results indicate that the Ge profile is constant over the Si-fins (as described in Fig. 2(a and b)).

It is important to emphasize here that if the dimensions (x, y and z) of the fins is comparable to the diffusion length of Si and Ge atoms with the present growth conditions then the kinetics represented by contribution of \( R^p \) term in Eq. (1) should be taken into account. In this case, the shape of the SiGe on Si fin could be very different from the present one in Fig. 2 or Fig. 3.

The Eq. (1) for the total growth rate is expressed in more detail as following:

\[
R_{\text{Total}} = \beta \left( 1 - \theta_{\text{HSi}} - \theta_{\text{ClSi}} \right) \frac{P_{\text{SiH}_2\text{Cl}_2}}{N_0} \left( \frac{E_{\text{SiH}_2\text{Cl}_2 \text{on Si}}}{k_b T} + 1 \right) \frac{P_{\text{GeH}_4}}{N_0} \left( \frac{E_{\text{GeH}_4 \text{on Si}}}{k_b T} + 1 \right) \frac{1}{\left( 1 + m_r \right) \left( 1 + \frac{\beta (\text{BP}_{\text{GeH}_4 \text{on Si}}) \ln \left( \frac{1}{2} \right)}{k_b T} \right)} \times \exp \left( \frac{E_{\text{GeH}_4 \text{on Si}}}{k_b T} \right) \times \left( \frac{1 + m_r}{1 + \frac{\beta (\text{BP}_{\text{GeH}_4 \text{on Si}}) \ln \left( \frac{1}{2} \right)}{k_b T}} \right) \times \left( \frac{1}{1 + \frac{\beta (\text{BP}_{\text{GeH}_4 \text{on Si}}) \ln \left( \frac{1}{2} \right)}{k_b T}} \right) \times \exp \left( \frac{-E_{\text{GeH}_4 \text{on Si}}}{k_b T} \right) \times \exp \left( \frac{0.1 \text{ eV}}{k_b T} \right) \times \exp \left( \frac{-E_{\text{etching}}}{k_b T} \right) - \frac{1}{N_0} \frac{p_{\text{HCl}}}{\left( 2\pi m_{\text{HCl}} k_b T \right)^{3/2}} \left( \frac{E_{\text{etching}}}{k_b T} + 1 \right) \exp \left( \frac{-E_{\text{etching}}}{k_b T} \right)
\]

where \( \theta \) parameters stand for the occupied dangling bonds (in presence of H and Cl) on Si with a specific surface orientation where \( N_0 \) is the number of atoms in unit volume for Si. \( E \) and \( P \) are activation energy and partial pressure for different reactant molecules, respectively. The variable “c” is the exposed Si coverage on the chip and B is a unit-less constant which is dependent on the architecture of the mask (oxide or nitride). The equation constants: \( \beta, \chi \) and \( \gamma \) are tooling factors which depend on the temperature distribution and gas kinetics over the susceptor in the CVD reactor.

A Si-fin has a shape where (001) plane is located at the central part and (111) planes at the sides. The \( \theta \) parameter has to be calculated for each orientation plane in Eq. (2).

The third term in the right side of the above equation which contains the exposed Si coverage, \( c \), in the pre-exponential coefficient relates to the pattern layout. In this term, an extra energy term of 0.1 eV has been added to the germane activation energy due to the diffusion of germane species on the oxide surface.

During the growth, the presence of germane atoms has a key role in increasing the number of free dangling bonds. In Eq. (2), \( m_r \) is a reaction related factor and is estimated to be 2.

The Ge content in the SiGe layers is obtained from a ratio of Si and Ge partial pressures according to [15]:

\[
\frac{x^2}{1-x} = 1.88 \times 10^{-4} \exp \left( \frac{E}{k_b T} \right) \frac{P_{\text{GeH}_4} + 5 \times 10^{-4} P_{\text{GeH}_4} \ln \left( \frac{1}{2} \right)}{P_{\text{SiH}_2\text{Cl}_2} - P_{\text{HCl}}} (3)
\]

where \( x \) and \( \lambda \) are the Ge content and reaction ratio, respectively. \( \lambda \) is related to the fraction of Cl atoms which interact with Si and Ge atoms. The \( \lambda \)-value is 1 when \( P_{\text{HCl}} = P_{\text{SiH}_2\text{Cl}_2} \) and is 0.8 for higher HCl amounts. \( E \) is the activation energy for the reaction which is extracted to 0.697 eV for SiGe [15,9].

In an ideal case, the Si-fin arrays are repeated over the whole chip (or over a wafer) but there are areas where this uniformity is disturbed. As examples, there are local and global alignment marks on each wafer or between the chips exist more oxide area.

Fig. 7 shows a schematic view of a mask layout which was used for SiGe growth calibration. A certain color in the figure presents a specific exposed Si area (the term \( c \) in Eq. (1)) where the density and size of Si-fins were constant. This chip was divided into two regions (light and dark blue which are region 1 and 2, respectively) in this figure. There are also other areas which contain alignment marks and test structures. It is important to mention here that fins in region 1 have more oxide around them compared to region 2. Table 1 shows the information for these regions and the results of calculated and measured SiGe layer profile for them. The measured Ge content comes from EDS analysis and the growth rate is calculated from the layer thickness estimated from HRSEM micrographs. However, as shown in Fig. 1(a), the exposed Si coverage of the (111) facets is not the same as (001) planes. Considering the trapezoid shape of the fins, one can estimate 7 times more exposed Si coverage for (111) facets compared to (001) planes on the top side of the trapezoid. Moreover, the surface atomic density on (111) facet is 7.8 × 10^{14} \text{ cm}^{-2} compared to 6.8 × 10^{14} \text{ cm}^{-2} for (100) planes. Considering these two factors, Table 1 shows the calculated and measured values for the fins located in regions 1 and 2.

These two areas of the chip make a non-uniform consumption of molecules and species over a chip. In principle, an array with large coverage of exposed Si area acts as a stronger attraction force – compared to the surrounding regions – for incoming reactant molecules. Thus, an interaction is established between the forces exerted on the molecules from the regions of a chip. Therefore, the growth rate over a region under such interactions is expressed as following [8]:

\[
R_T(d) = R_A + \left( R_{\text{sur}} - R_A \right) \left( 1 - e^{-\alpha d} \right)
\]
where $d$ is the distance from the region of chip with large coverage of exposed Si area and $c_{surr}$ is the exposed Si coverage of the surrounding regions. In this equation, $R_A$ is the growth rate of an array with the highest exposed Si coverage in a particular part of the chip. This part has dominant role in consumption of incoming atoms (or traps most of the molecules) while $R_{surr}$ is the growth rate of arrays situated in the surrounding of this array. In the above equation, the exponential function determines the interaction between the regions of the chip. The variable $\tau$ is called interaction range and represents the length through which an array of Si-fins has interaction with its surrounding arrays. The $\tau$ variable has a central role in pattern dependency of the growth and it is defined as follows:

$$\tau = \frac{1}{2Kc + \beta K \sqrt{c} + \delta}$$

(5)

where $\alpha$ and $\beta$ are constants which refer to how far the movement of the molecules over the chip are affected by dangling bonds. In the above equation, $\delta$ is another kinetic constant which considers the collisions of the gas molecules before arriving to the dangling sites. If $\delta$ increases, the interaction range decreases due to the limited migration of the gas molecules on top of the chip.

Empirical calculations showed that the following are the most suitable values for the growth temperatures close to 650 °C for this model:

$K_x = 0.0004 \ \mu m^{-1} , \ \ K_y = 0.0011 \ \mu m^{-1} , \ \ K = 0.00048 \ \mu m^{-1}$

The main idea of the pattern dependency modeling is based on the non-uniform gas consumption among the chips. As shown in Figs. 2 and 3, the Ge content and thickness of SiGe layers was obtained by using EDS technique in HRSEM and cross-sectional images, respectively. The EDS technique was used to confirm the XRD results. Table 1 summarizes the calculated and measured data of the SiGe layers for the fins in Fig. 7.

The input parameters for calculation of the SiGe data in Table 1 are partial pressures of Si, Ge and HCl ($P_{Si}, P_{Ge}$ and $P_{HCl}$ are 15.99, 0.533 and 8.66 Pa, respectively) at $T = 650$ °C for two different values of exposed Si coverage (0.34% and 2.12%). The number of dangling bonds for (111) and (100) planes ($7.8 \times 10^{14} cm^{-2}$ and $6.8 \times 10^{14} cm^{-2}$, respectively) and the activation energies ($\sim 2.08$ eV for both of the planes) are input parameters for the calculations in Table 1.

The largest consumption of gas molecules occurs over the region with largest number of dangling bonds for $c_z = 2.12\%$ arrays

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**Table 1**

The calculated and measured SiGe profiles in regions 1 and 2 in Fig. 7. For the calculated growth rates both Eqs. (2) and (3) are used. The measured values are derived by HRSEM.

<table>
<thead>
<tr>
<th>Region</th>
<th>Exposed Si (%)</th>
<th>Calculated Ge content (%)</th>
<th>Measured Ge content (EDS) (%)</th>
<th>Calculated growth rate (nm/s) (100) &amp; (111)</th>
<th>Measured growth rate (100) &amp; (111) (nm/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.34</td>
<td>35.29</td>
<td>35.23</td>
<td>0.92 &amp; 0.54</td>
<td>0.85 &amp; 0.51</td>
</tr>
<tr>
<td>2</td>
<td>2.12</td>
<td>33.75</td>
<td>35</td>
<td>0.73 &amp; 0.43</td>
<td>0.71 &amp; 0.42 (see Fig. 8)</td>
</tr>
</tbody>
</table>

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Fig. 8. Cross-sectional TEM image of a fin in region 2 in Fig. 7. The calculated layer thickness is marked by dashed lines.

(where (1 1 1) planes absorb the most of gas molecules). In this case, the growth rate over C2 region is denoted by Rn in Eq. (4) while Rnom is related to the surrounding parts of chip. The interaction length, l, is calculated to 1541 μm and 1833 μm from Eq. (5) for C1 and C2, respectively. The growth rate (R) on any array of Si fins with a distance of “d” from C1 or C2 can be calculated from Eq. (4). Fig. 8 demonstrates the SiGe layer grown over a fin and the calculated layer thickness from Table 1. The calculated values for SiGe layer profiles are in good consistency with the measured values.

5. Conclusions

The integration of selective epitaxy of SiGe (0.33 ≤ x ≤ 0.35) in the source/drain regions was demonstrated for 14 nm node FinFET technology. The thermal budget was limited to temperatures in 780–800 °C range in order to preserve the Si-fin shape and grow SiGe layers with high epitaxial quality. The Ge profile in SiGe layers with low pattern dependency in selective epitaxy of B-doped SiGe layers for advanced metal oxide semiconductor field effect transistors. In: IEEE int electron devices meet 2003. p. 110–1. <http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=5331587>.

References


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