Integration of Ni$_2$Si/Si Nanograss Heterojunction on n-MOSFET to Realize High-Sensitivity Phototransistors

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Abstract—We report a top-down fabrication technique for direct integration of Ni$_2$Si/Si heterojunction arrays on n-type MOSFET gate terminal to realize sensitive field-effect phototransistors (PTs). It was observed that exposing gate area to light ($\lambda = 655$ nm) leads to significant modulation of threshold voltage ($V_{TH}$) of PT in comparison with a conventional MOSFET. By analyzing optical absorption spectra of Ni$_2$Si/Si nanostructures on SiO$_2$ of this novel PT and planar Ni$_2$Si/poly-Si on SiO$_2$ of conventional transistors, we concluded that, nanostructures strongly improve light absorption. This results in higher optically generated electron–hole pairs in which excess holes induce an electric field on the transistor channel and help the threshold happen at lower voltages. To recognize the appropriate operating point of such nanostructure-based PT, effect of $V_{GS}$ on the sensitivity of drain current was investigated. Experimental results show that device sensitivity ($S$) is related to gate–source voltage via a homographic like function. Theoretical analysis shows $S \propto 1/(V_{GS} - V_{TH})$ for high $V_{GS}$, which has been confirmed by experimental data. In addition, external quantum efficiency and photoresponsivity of PT as functions of gate voltage were studied. The achieved results suggest that this device would be a promising candidate for fabricating low-power PTs based on silicon nanostructures.

Index Terms—Electro-optical properties, nickel silicide, optical absorption, phototransistor (PT), silicon nanograss.

I. INTRODUCTION

ONE DIMENSIONAL (1-D) and quasi-1-D nanostructures can consistently offer fascinating physical properties that are not observed in the bulk counterpart [1]–[3]. Owing to the ongoing advancements in the growth and fabrication methodologies, these nanomaterials find their way in various fields of research including health science, energy conversion and storage, and low power electronics [4]–[6]. Furthermore, one of the most studied phenomena in nanostructures is their observable sensitivity to light that could be expected to meet emerging technological demands.

In this context, optical devices based on array of 1-D silicon nanostructures have been widely investigated, particularly for photodetection at visible wavelengths [3]. Sensitivity of these devices is strongly dependent on their effective photosensitive area. However, with the continued scaling rules, the sensitivity of devices has decreased as most of the die area is taken over by peripheral circuitry and reducing the detecting area. It is believed that utilizing phototransistors (PTs) minimizes the need for preamplification allowing larger area photosensitive devices. Also in PTs, attaining higher sensitivity and responsivity (the ratio of photocurrent to dark current and incident light intensity, respectively) are more feasible. This is because gate voltage ($V_{GS}$) can autonomously affect photocurrent, regardless of the incident light intensity. There are reports on fabrication of PTs based on single 1-D nanostructures [3], [8]–[11] which mainly applied as probes for investigating the unique physical properties of low-dimensional systems. However, they usually suffer complicated and low-yield fabrication processes make them rarely compatible with the complementary metal–oxide–semiconductor (CMOS) technology.

In this paper, direct integration of Ni$_2$Si/Si nanograss heterojunction arrays on a MOSFET’s gate terminal has been applied to realize a sensitive PT based on a CMOS compatible top–down technique. The integrated nanostructures found to be convenient for boosting optical absorption that consequently lead to higher photogeneration of electron–hole pairs (EHPs) and causing a significant modulation of threshold voltage ($V_{TH}$). Measurements reveal that for a fixed intensity of incident light, PTs sensitivity can be adjusted by tuning bias voltage ($V_{GS}$) that has been supported by our theoretical analysis. In addition, quantum efficiency (QE) and photoresponsivity with values in excess of 10% and 62 mA/W were detected.

II. EXPERIMENTAL METHODS

A. Silicon Nanograss Formation

An array of Ni-silicide/Si heterojunction has been realized by a multistep process on n-type silicon (100) substrates. By means of a reactive ion etching (RIE) system Si-nanograsses are fabricated in an RF plasma (13.56 MHz) environment composed of O$_2$, H$_2$, and SF$_6$ gasses with...
substrate [Si (004)]. The sharp peak at \(2\theta = 69.7\)° is due to the crystalline silicon substrate [Si (004)].

The silicon substrate is loaded into an annealing furnace and heated up to 750 °C in a dry oxide furnace [Fig. 3(c)]. Then, Si-nanograsses in the surrounding area were etched away by directional SF6 plasma at pressure of 150 mtorr. This silicon layer is exploited to construct Si-nanograss on the gate terminal utilizing the same procedure mentioned above [Fig. 3(b)]. Indeed, the passivation/etching steps repeated as many cycle as needed to ensure that the whole layer is converted to the desired nanostructures. The SiO2 layer beneath the poly-Si acts as the etch stop layer in this step. Afterward, a thin layer of nickel was deposited on the surface of the sample and then was patterned to define the gate region [Fig. 3(d)]. Next step is definition of source, drain, and channel regions [Fig. 3(e)]. After removing oxide layer in the demarcated area through sequential lithography, optical, and mechanical properties of devices based on silicon nanostructures. Deposition of thin layer of nickel with an approximate thickness of 15 nm on the surface of Si-nanograsses using an electron beam evaporator is the next step in the construction of the following heterojunction. Afterward, the sample was loaded into an annealing furnace and heated up to 750 °C in argon ambient for 20 m. Then, the residual nickel on the sample was stripped off with nickel etchant composed of 3C6H8O7/H2SO4/5H2O solution.

X-ray diffraction (XRD) pattern of the array of heterojunctions is shown in Fig. 2. Sample was characterized using Philips XPERT PRO system with Cu Kα (\(\lambda = 0.154060\) nm) radiation to identify Ni-silicide phases present. Observed peaks located at \(2\theta = 32.48, 42.38,\) and 48.76 reveal that among most probable stable phases (Ni5Si2, NiSi, and NiSi2) [12], annealing of our Ni–Si binary system at 750 °C concludes formation of Ni2Si phase. It should be kept in mind that Ni2Si is the very first stable phase forms while, in the case of thin Ni layer, transition to NiSi phase does not occur, or at least does not become observable at the Ni2Si/Si interface as long as the deposited Ni is not totally exhausted [2, 7, 13]. Therefore, the only phase detected in the XRD spectra is Ni2Si. The intense peak located at \(2\theta = 69.7\)° is the intrinsic characteristics of silicon substrate.

**B. Fabrication of PT**

Wafer cleaning using standard RCA#1 solution is the first step in fabrication of PT. Then, sample was inserted into a dry oxide furnace (1100 °C) for the growth of approximately 70-nm silicon dioxide (SiO2) as the gate dielectric. Subsequently, sample was loaded into a low-pressure chemical vapor deposition chamber for deposition of a thick layer of polycrystalline silicon [Fig. 3(a)]. Poly-Si deposition was performed at temperature of 620 °C while silane (SiH4) serves as silicon agent and hydrogen (H2) as carrier gas at total pressure of 10 torr. Typical thickness of poly-Si is approximately 800 nm. This silicon layer is exploited to construct Si-nanograss on the gate terminal utilizing the same procedure mentioned above [Fig. 3(b)]. Indeed, the passivation/etching steps repeated as many cycle as needed to ensure that the whole layer is converted to the desired nanostructures. The SiO2 layer beneath the poly-Si acts as the etch stop layer in this step. Afterward, a thin layer of nickel was deposited on the surface of the sample and then was patterned to define the gate area by means of standard photolithography processes and Ni etching [Fig. 3(c)]. Then, Si-nanograsses in the surrounding area were etched away by directionalf SF6 plasma at pressure of 2.5 torr using RIE machine to assure that nanostructures only exist on the gate terminal [Fig. 3(d)]. Next step is definition of source, drain, and channel regions [Fig. 3(e)]. After removing oxide layer in the demarcated area through sequential lithography and etching (with buffer HF 10% solution) steps, active regions are determined. Transistor was designed to have channel length and width of 150 and 250 \(\mu\)m, respectively. The final step is simultaneous introduction of dopant to the
active area and formation of Ni-silicide at the top of the gate electrode [Fig. 3(f)]. Both of these events occur in the phosphorous doping furnace at 750 °C to add n-type dopants into the active regions and anneal Ni–Si system to form nickel silicide on the gate designated area. At the end of integration processes, the residue of pristine Ni was etched away. Outline of fabrication steps is shown in Fig. 3. SEM image of the obtained heterojunctions on the gate [inset of Fig. 3(f)] shows that tip of the nanograsses are a bit round. Thermal annealing at fairly high temperature and dipping in HF solution might cause this phenomenon.

C. Optical Tests

To explore the usefulness of designed device as a PT, the integrated nanostructures on top of the gate area were illuminated by a monochromatic red light laser diode (λ ∼ 655 nm). This is accomplished by coupling the light into a multimode fiber optic with the approximate core diameter of 125 μm to assure that source/drain regions are not exposed to the incident light. For the sake of comparison, a conventional transistor (with a planar gate platform of Ni2Si/poly-Si/SiO2 stack) with the same geometrical dimension (W and L) was also experimented to investigate the importance of integration of nanostructures onto the gate terminal.

III. RESULTS AND DISCUSSION

Fig. 4(a) and (b) comparatively depicts both nanostructure covered and conventional transistors transfer characteristics (ID–VGS) at the presence and absence of irradiation. The ID–VGS curve, in the presence of Ni2Si/Si nanostructures [Fig. 4(a)], reveals that illumination of gate area leads to modulation of threshold voltage (VTH) that consequently increases the drain current. A fairly significant change in the threshold voltage from 0.71 to 0.49 V due to light illumination is observed for the PT, meanwhile no changes were detected for the conventional one [Fig. 4(b)]. To elaborate the mechanism, a schematic is shown in Fig. 4(c). The incident light generates free EHPs in the Ni2Si/Si nanostructures. In the presence of gate electric field, the photogenerated electrons are easily collected by the gate electrode that provides gate voltage.

On contrary, the photogenerated holes through a drift process reach the nanostructures/SiO2 interface [Fig. 4(c), right]. The Ni2Si/SiO2/Si stack behaves like a parallel plate capacitor. Therefore, accumulation of holes calls for corresponding net negative charges at the surface of semiconductor. Such negative charges in a p-type material arise from depletion of the holes from the region near the surface, leaving behind uncompensated ionized acceptors. Equation (1) shows threshold voltage expression of a conventional MOSFET

\[ V_{TH} = -\frac{Q_d}{C_i} + 2\phi_F. \]  

In this expression, \( Q_d, C_i \), and \( \phi_F \) are depletion charges, insulator capacitance per unit area, and difference between the bulk and intrinsic Fermi levels, respectively. The light exposure of gate area does not affect \( \phi_F \), because it is an inherent characteristics of utilized silicon wafer. Therefore, we can write an expression for threshold voltage changes as

\[ \Delta V_{TH} = -\frac{\Delta Q_d}{C_i} = -\frac{Q_{dp}}{C_i}. \]  

Since \( Q_d \) is positive, \( \Delta V_{TH} \) is negative. In other words, optically generated holes exert an electric field on the underlying insulator and subsequently on the channel region, which in turn promote channel depletion and inversion at a smaller bias voltage. As Fig. 4(b) shows, light exposure did not alter transfer characteristics of the conventional transistor. Therefore, the threshold voltage does not change significantly.

It is speculated that weak optical absorption of incident light by the gate poly-Si plays a major role. Therefore, optical absorption spectra of array-of-heterojunction/SiO2/Si and stack of planar Ni2Si–Si/SiO2/Si are comparatively shown in Fig. 5. Heterojunction covered sample absorbs more than 98%
of the incident light with wavelengths around $\lambda = 655$ nm, whereas the absorption is less than 30% for the other sample. Indeed, effects arising from the low dimensionality including enhanced light scattering, waveguiding effects (light tunneling), and larger surface to volume ratio boost optical absorption of the sample decorated with nanostructures [11]. This reflects that the concentration of photogenerated EHPs in planar structure is not enough to effectively modulate threshold voltage and consequently drain current. The oscillatory behavior in optical absorption corresponding to planar sample is due to the multiple internal reflections from poly-Si/SiO$_2$ and SiO$_2$/Si interfaces [14].

Fig. 6(a)–(f) illustrates output characteristics ($I_D$–$V_{DS}$) of fabricated PT for various $V_{GS}$, which exhibit classical linear/saturation behavior. As seen, for lower gate biases, the relative increment in drain current due to the light illumination is more considerable. To study the effect of gate voltage on the changes of $I_D$, the relative sensitivity of the PT at different $V_{GS}$ is defined as

$$S = \frac{I_{\text{irradiated}} - I_{\text{dark}}}{I_{\text{dark}}}.$$  

(3)

For ease of calculation, saturation currents at $V_{DS} = 5$ V are used for both dark and irradiated conditions. The histogram of Fig. 6(g) shows the variation in the measured sensitivity with respect to the biasing voltage of transistor. Apparently, lower $V_{GS}$ for a constant intensity of light, provide higher sensitivity as a well-desired prospective in low-power photodetecting application.

The output drain current of a long channel MOSFET operating in the saturation region is expressed as

$$I_D = \frac{W}{2L} \mu C_{ox}(V_{GS} - V_{TH})^2 \left(1 + \frac{V_{DS}}{V_A}\right).$$  

(4)

For a fixed light intensity, the concentration of optically generated excess EHPs is fixed. However, it is speculated that increasing $V_{GS}$, gradually, will screen the effect of these excess carriers aggregated at the nanostructure/SiO$_2$ interface, which reduces device sensitivity. To further elaborate the origin of this behavior in the PT sensitivity theoretical calculation is presented. Assuming that $\Delta V_{TH}$ happens due to the light illumination, then exploiting (4), we can write a general expression for the net change of $I_D(\Delta I_D)$

$$\Delta I_D = \frac{1}{2} \frac{W}{L} \mu C_{ox} \left[\Delta V_{TH}^2 + 2\Delta V_{TH}(V_{GS} - V_{TH})\right] \left(1 + \frac{V_{DS}}{V_A}\right).$$  

(5)

Using (3) we have

$$S = \frac{\Delta V_{TH}^2 + 2\Delta V_{TH}(V_{GS} - V_{TH})}{(V_{GS} - V_{TH})^2}.$$  

(6)

Equation (6) reveals that for high gate voltages, $S$ inversely relates to $V_{GS}$, i.e., $S \propto 1/(V_{GS} - V_{TH})$, which confirms the experimentally observed behavior. The external QE of the PT, as a measure of device electrical sensitivity in response to incident light, also can be estimated as follows:

$$Q.E = \frac{\Delta I_D}{I_{inc}} \times \frac{h \cdot c}{\lambda} \times \frac{1}{P_{inc}}.$$  

(7)

where $\Delta I_D = I_{\text{irradiated}} - I_{\text{dark}}, P_{inc}, e, h, c$, and $\lambda$ are drain current change after illumination, incident light power (1 mW), electron charge, Planck constant, speed of light, and wavelength of the light, respectively. In (7), $\Gamma$ is a weighting factor that accounts for recombination of the optically generated EHPs in the gate region. Considering higher mobility of electrons compares with that of holes, it is shown that $\Gamma$ is as follows [15]:

$$\Gamma = \mu_{\text{poly}} \frac{V_{GS}}{L_{\text{poly-Si}}} r.$$  

(8)

In this expression, $\mu_{\text{poly}}, L_{\text{poly-Si}}$, and $r$ are electron mobility, effective thickness of the polycrystalline silicon gate region, and carriers’ recombination lifetime, respectively. Lipson’s group has shown that due to existence of grain boundaries, EHP recombination lifetime in polycrystalline silicon is approximately 150 ps [16]. Furthermore, the electron mobility in the polycrystalline silicon is about 8–9 cm$^2$/V·s [17]. Based on this information, QE of the PT as a function of gate voltage is obtained and plotted in Fig. 7 (black curve). It is observed that QE decreases with increasing the gate voltage with largest QE of more than 10%, which is comparable with [18]. To elaborate more on the sensitivity of the device, we calculated the photoresponsivity, defined as
the ratio of the photocurrent (i.e., $\Delta I_P$) to the input power ($\Delta I_P / P_{inc}$). The red curve in Fig. 7 shows responsivity with respect to the bias voltage that discloses a fairly noticeable maximum of 62 mA/W at $V_{GS} = 2.5$ V. The detected trends in photoresponsivity and QE of our PT are in complete agreement with those reported in [18] and [19] in which photoresponse in biased photodetector is predominated by photovoltaic and photooinduced bolometric effects, while the thermoelectric effect is insignificant. The variation of $S$, QE, and photoresponsivity with the bias voltage opens up an opportunity for tuning transistor’s operating point to simultaneously achieve high sensitivity to light as well as sustaining an acceptable noise safety margin.

IV. Conclusion

In summary, exploiting a convenient top-down technique, Ni$_2$Si/Si nanograss heterojunction were integrated on a MOSFET gate terminal to fabricate a sensitive PT by enhancing the optical absorption. It was shown that by monitoring threshold voltage or drain saturation current, the incident light on the gate area can be detected. Tuning of QE, photosensitivity, and relative sensitivity of the device with respect to the $V_{GS}$ was also studied. The outcomes showed gate voltage acts as a knob allows tailoring device performance for photodetection applications.

References


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