Design of a direct conversion ultra low power ZigBee receiver RF front-end for wireless sensor networks

Mohsen Javadi*, Samad Sheikhaei, Aazar Saadaat Kashi, Hossein Pourmodheji

School of Electrical and Computer Engineering, College of Engineering, University of Tehran, Tehran, Iran

**Article info**

Article history:
Received 12 February 2012
Received in revised form 1 November 2012
Accepted 14 November 2012
Available online 7 December 2012

Keywords:
ZigBee
LMV cell
LV cell
Wireless Sensor Networks
Direct conversion
Ultra low power

**Abstract**

This paper describes an ultra low power receiver RF front-end to be utilized for wireless sensor network (WSN) applications. The design of the LV cell (LNA and VCO) that is proposed in this paper is suitable for direct conversion architecture, while the conventional LMV cell (LNA, Mixer, and VCO) is used only in low-IF architectures, due to the prohibitive high flicker noise. A passive mixer is utilized instead of an active mixer and a capacitor is added to block the DC current flowing into the mixer. So, flicker noise corner frequency is reduced to 13.8 kHz. The proposed design can be used more easily compared to conventional LMV cell in a low voltage technology, because of the stacking of only two blocks (LNA and VCO), while three blocks of LNA, mixer, and VCO are stacked in the conventional LMV cell. The proposed receiver RF front-end consumes 1 mW in 0.18 μm CMOS technology with a 1.2 V supply source. NF and IIP3 are 4.7 dB and −7 dBm, respectively.

© 2012 Elsevier Ltd. All rights reserved.

1. Introduction

Wireless Sensor Network (WSN) is a new concept that utilizes a large number of nodes or sensors the role of which is to control an event or collect information from an environment [1]. The nodes may not be accessible for battery replacement in a WSN. So, it is important that their power consumption is reduced to make sure they can operate for a long time on a single battery [2]. ZigBee standard has been defined for low data rate, low power consumption, and low cost applications and these are the reasons ZigBee is used in WSN. Today, ZigBee standard is frequently used in military and industry applications, because of high security, low cost and low power consumption.

Different ways such as current reuse technique in [2–4] and supply voltage reduction are used to reduce power consumption. Ultra low supply voltage reduces “supply-to-threshold-voltage-ratio” that creates various problems in the design of RF circuits. These problems result from cut off frequency reduction in CMOS technology by the ultra low supply voltage [5]. By applying this method and current reuse technique, the total power consumption can be reduced. However, in this paper we discuss applications that use low voltage (not ultra low voltage), so those problems are avoided here.

LMV (LNA, Mixer, VCO) cell topology which uses the current reuse technique is presented in [6] for the first time. RF blocks, including low noise amplifier (LNA), mixer, and voltage controlled oscillator (VCO) are stacked and they use a common bias current. In [6], this structure is designed for a low-IF architecture receiver for the GPS standard. LMV cell is also used for a ZigBee standard receiver in [3] that resulted in reduction of power consumption. But in those designs, IIP3 is low due to the stacking of three blocks. Also, because of the use of an active mixer that has high flicker noise, LMV cell cannot be used for direct conversion receivers. A modification to the LMV cell is proposed in this paper that is made by stacking LNA and VCO, while three blocks of LNA, mixer, and VCO are stacked in the conventional LMV cell. The proposed receiver RF front-end consumes 1 mW in 0.18 μm CMOS technology with a 1.2 V supply source. NF and IIP3 are 4.7 dB and −7 dBm, respectively.

The rest of the paper is organized as follows. In Section 2, system level requirements for the ZigBee standard are described. The proposed design is explained in Section 3. Section 4 summarizes the simulation results of the receiver RF front-end, and Section 5 draws the conclusions.

2. Receiver system design

Some parameters for designing a receiver are NF and IIP3 that are obtained from ZigBee standard specs. Extraction of these parameters is described in this section.
2.1. Noise figure

Fig. 1 shows bandwidth, channel spacing, and signal power of the adjacent channels in the 2.4 GHz ZigBee physical layer [3]. This figure shows signal strength versus offset frequency from the center of the channel of interest. The IEEE 802.15.4 PHY standard requires 0 dB tolerance to an adjacent channel blocker and 30 dB tolerance to an alternate channel blocker.

The packet error rate (PER) in the receiver that represents the receiver performance should be less than 1%. The number of bits per packet is about 20 bytes or 160 bits. Therefore, 1% PER is equal to 0.00625% bit error rate (BER) [7]. The IEEE 802.15.4 2.4 GHz PHY layer uses DSSS O-QPSK with half sine pulse modulation. The simulated BER curve of an O-QPSK and a DSSS O-QPSK versus SNR is plotted in Fig. 2. This curve is achieved by a system level simulation. As shown in Fig. 2, an O-QPSK modulation needs a minimum SNR of about 8.5 dB for 0.00625% BER as required by the standard, while a DSSS O-QPSK modulation only needs 0.5 dB SNR. This improvement in required SNR is due to process gain that is the result of Direct-Sequence Spread Spectrum (DSSS) technique, which is defined for more security in the ZigBee standard.

Noise floor \( P_N \) of a receiver without noise is calculated by (1) [8].

\[
P_N = -174(\text{dBm/Hz}) + 10\log(\text{BW})
\]  

(1)

In this equation, BW is the signal bandwidth. The channel select filter bandwidth is 1 MHz for a direct conversion receiver. By adding values in (1), the noise floor is achieved as \(-114\) dBm. The minimum SNR for a DSSS O-QPSK modulation that is calculated above is 0.5 dB. Therefore, the minimum signal power should be \(-113.5\) dBm. The receiver sensitivity in the standard is \(-85\) dBm, so the NF of the receiver front-end should be less than 28.5 dB. Assuming an 8.5 dB implementation margin, which accounts for board losses (external component losses and digital losses in the receiver) [9], the maximum NF is equal to 20 dB.

2.2. Linearity

The nonlinearity requirements can be inferred from the interferer profile and jamming tolerance requirements, and so, the IIP3 requirement is calculated by [9]

\[
\text{IIP}_3 > \left( \frac{3P_{\text{int}} - P_{\text{sig}} + \text{SNR}_{\text{min}} + \text{Margin}}{2} \right)
\]

(2)

where \( P_{\text{int}} \) is the power of two interferences at \( \pm 10 \) MHz and \( \pm 20 \) MHz. Also, \( P_{\text{sig}} \) shows the main signal power. By considering \( P_{\text{sig}} = -82 \) dBm, 3 dB more than the required sensitivity, \( \text{SNR}_{\text{min}} = 0.5 \) dB, and \( \text{Margin} = 10 \) dB, the maximum value of IIP3 is calculated as \(-28\) dBm.

The maximum input power of the receiver in the ZigBee standard is \(-20\) dBm. So, the receiver 1 dB compression point, for this input power, should be larger than \(-20\) dBm. IIP3 is usually 10 dB more than the 1 dB compression point [8]. So IIP3 for high input power is about \(-10\) dBm. The receiver requirement is summarized in Table 1.

3. The proposed receiver topology

Super-heterodyne, direct conversion and low-IF are conventional architectures in designing RF circuits. The super-heterodyne receiver is more popular than other architectures due to high gain, more flexibility in design and good I/Q matching. However, this architecture cannot be used for ZigBee applications, due to a relatively large number of off-chip components, such as a SAW filter. Also, it suffers from high power consumption, high cost of implementation, and image rejection problem. The low-IF architecture can be implemented at a low cost. This architecture consumes lower power than super-heterodyne structure, but it needs a relatively high-Q image reject filter circuit, which adds to the complexity and therefore power consumption and chip implementation area, compared to zero-IF architecture [1]. Therefore, zero-IF architecture is chosen for the proposed receiver circuit.

Zero-IF architecture has two major issues: flicker noise, and DC offset. However, the ZigBee signal spectrum has a notch at DC, and thus the flicker noise and DC offset can simply be removed without destruction of the information in the signal [1]. Utilizing a common current to bias receiver blocks is a good method for reducing power consumption. Fig. 3 shows a simple circuit of a LMV cell. As shown in the picture, all of the RF blocks including LNA, mixer, and VCO, are stacked and use a common current. Depending on IF load, the topology can be implemented in current mode or voltage mode. If virtual ground, which is described in Section 3.4, is chosen for the output load, the LMV cell acts in current mode. As explained in [6], this topology has better results than voltage mode that is implemented by a high impedance load at the LMV cell output.

<table>
<thead>
<tr>
<th>Table 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Summary of the receiver specification.</td>
</tr>
<tr>
<td>Rx Block</td>
</tr>
<tr>
<td>Noise figure</td>
</tr>
</tbody>
</table>
| IIP3 | For max gain: \( \text{IIP}_3 > -28 \) dBm 
For min gain: \( \text{IIP}_3 > -10 \) dBm |
| Input power | \(-85 \) to \(-20 \) dBm |
It is difficult to stack the blocks when supply voltage is reduced. On the other hand, the LMV cell has high flicker noise, because the mixer block has high DC current. A passive mixer can be used to achieve a low flicker noise receiver structure. The mixer is therefore taken out of the LMV cell to implement this idea, in this paper. Thus, just LNA and VCO blocks are stacked and the low supply voltage problem is alleviated. In this topology, IIP3 is improved due to the increase of the output swing. The proposed LV cell is shown in Fig. 4.

The operation of the circuit in current mode increases linearity [5]. A parallel LC filter is used at the interface of LNA and VCO blocks to make sure that the RF components in the output current of LNA do not flow into the VCO, and instead go to the LNA output (i.e., the LV cell output). Therefore, VCO and LNA are separated at 2.4 GHz. Adding this filter between LNA and VCO has two advantages:

1. It prevents reduction of the conversion gain.
2. It reduces the chance of the LO pulling by the LNA.

The first advantage is achieved as the output current of the LNA is completely directed into the mixer. The second advantage is achieved as no part of the LNA ac current goes into the VCO. Therefore, LO pulling does not happen in the VCO.

Capacitor $C_f$ is added as a dc current blocker in the LNA output current path to reduce flicker noise. A passive mixer that has low flicker noise is located after the LV cell.

### 3.1. LNA

Common gate (CG) and common source (CS) topologies can be used to design a LNA. A CG topology provides a higher matching bandwidth compared to the CS stage, but it has a higher NF as well [2]. For the given narrow bandwidth of ZigBee standard, therefore, CS LNA is a suitable candidate.

The input matching circuit is shown in Fig. 5. The input impedance is obtained from (3) [8]. In this equation, $g_{in}$ is transconductance of the LNA transistor. Resonance frequency of the matching circuit ($\omega_0$) is equal to the resonance frequency of the capacitance and sum of the two inductors. Thus, by adjusting the inductor and capacitor for resonance at the desired operating frequency, only the third term of (3) remains which shows the resistance that is seen in this frequency, and should be made equal to the impedance of the antenna ($R_s$). Adding $L_g$ gives an additional degree of freedom to set $\omega_0$ and $R_s$, independently.

$$Z_{in} = \frac{1}{sC_{gs}} + s(L_g + L_{deg}) + \frac{g_{in}}{sC_{gs}}L_{deg}$$

Also, Q of the matching circuit is calculated from (4).

$$Q = \frac{(L_{deg} + L_g)\omega_0}{2R_s}$$

Fig. 3. Conventional LMV cell [13].

Fig. 4. The proposed receiver topology (LV cell, Mixer and Virtual Ground).
Eq. (5) shows voltage gain of the LNA,

$$A_V = Q \frac{g_m R_{out-LNA}}{C_0}$$  \hspace{1cm} (5)

where $R_{out-LNA}$ is the output resistance that is seen at the load of LNA at the operating frequency. According to (5), with increasing $Q$, the voltage gain of the first stage of the receiver will be increased. So the noise of the next stages would have lower effect. Therefore, NF reduces with increasing $Q$. On the other hand, by increasing the gain of LNA (by a higher $Q$) and thus raising output amplitude for a given input voltage, receiver linearity will be reduced. So there is a trade-off between $Q$ and linearity, that should be considered for choosing $Q$. Fig. 6 shows the S11 curve for 50 $\Omega$ impedance matching.

3.2. QVCO

A direct conversion requires quadrature downconversion in order to avoid the signal corrupting itself in the baseband. Either RF or LO signals can be made in quadrature, for this purpose. In the RF path, 90 degree phase shift is usually generated by passive blocks. So, extra power consumption is not imposed to the design, but it causes attenuation and distortion in the RF signal, and this technique, on the other hand, has low accuracy in I/Q matching. Thus, signal may require correction in the baseband for compensation of the I/Q mismatches. The alternative to this is to generate quadrature signals by a quadrature LO or in the LO path using an active block. This method usually consumes more power due to the use of active blocks, but has high accuracy in I/Q matching.

There are several schemes to generate quadrature signals in a LMV cell. A common method is to create an oscillation with twice the required frequency and using a frequency divider. This method has high matching accuracy for quadrature signals, but use of the divider block leads to extra power consumption. Another solution is to use source injection or drain injection topologies to create a quadrature oscillator in the LMV cell. In [6], drain injection topology to generate quadrature signals is used. This method requires another bias current for injection into the oscillators and therefore leads to somewhat more power consumption. The topology, which is used in this paper, is source injection method [10]. This method generates quadrature signals with no need for an extra bias current. Also, as reported in [10], source injection topology has lower phase noise than drain injection topology.

3.3. Mixer

A passive mixer is used in this design due to the lower flicker noise compared to active mixers. Also, by utilizing a passive mixer in the current mode, the mixer has a lower loss than a passive mixer which works in the voltage mode. Flicker noise has an inversely proportional relation with the transistor channel length and width. Therefore, increasing the size of the mixer transistors can reduce flicker noise, but it also reduces conversion gain, due to the added parasitic capacitance. This will be discussed more, later.

By assuming a high impedance for the LC tank at 2.4 GHz compared with impedance that is seen from the mixer input in the LNA output node, the input current of the mixer is obtained by dividing the LNA output current between the mixer resistance and parasitic capacitor impedance in the source of the mixer, that is shown by (6). Therefore, equivalent drain-source resistance should be lower than parasitic capacitor impedance at 2.4 GHz.

$$\frac{I_{DS}}{I_{ge}} = \frac{1}{1 + RC_{p(LO)}}$$  \hspace{1cm} (6)
In this equation, $I_{DS}$ is the current of mixer drain-source channel and $R$ is its resistance, and $C_P$ is the parasitic capacitor in the mixer source. As shown by (7) and (8), parasitic capacitance of a transistor is proportional to the channel length and width, while drain-source resistance of a transistor in the triode region is proportional to the channel length and inversely proportional to the channel width.

$$R \propto \frac{1}{\mu C_{ox}(W/L)V_{od}} \quad (7)$$

$$C_P \propto WLC_{ox} \quad (8)$$

$$R_{CP} \propto \frac{L^2}{\mu V_{od}} \quad (9)$$

In (9), $V_{od}$ is the overdrive voltage that is equal to $(V_{GS} - V_t)$. Based on (6) and (9), the width of transistors in the passive mixer has no effect on the conversion gain. But the conversion gain is inversely proportional to the square of channel length if $RC_{p} \ll 1$. Therefore, the channel length is chosen at the minimum length that the technology allows. Increasing the width of the transistor reduces the equivalent resistance seen at the mixer input and reduces voltage gain of the LNA. The input noise power of the mixer referred to as the input of LNA is given by:

$$P_{n,MIXER|LNA input} = \frac{P_{n,MIXER}}{A^2_{0,LNA}} \quad (10)$$

Using a large transistor reduces flicker noise; however, width of the mixer transistors should not be chosen very large, as it reduces the equivalent resistance at the output of LNA and therefore the voltage gain of LNA, which affects the overall NF.

### 3.4. Virtual ground

A trans-impedance amplifier (TIA) converts the low frequency conversion current of the mixer to voltage. A TIA works as a virtual ground block that is shown in Fig. 7. This topology is taken from [3]. The input impedance at low frequency is obtained from (11).

$$Z_{\text{in-diff}} = \frac{2}{g_{m1,2}A_0} \quad (11)$$

In this equation, $g_{m1,2}$ is the transconductance of transistors $M_1$ and $M_2$, and $A_0$ is the DC gain of the core amplifier. $R_1$ and $R_2$ are used to create a bias current path for feedback transistors ($M_1$ and $M_2$). For a given bias current, $g_{m1,2}$ can be increased by choosing a larger aspect ratio for the two transistors $M_1$ and $M_2$. A higher transconductance for transistors $M_1$/$M_2$ can be obtained by increasing their bias current, at the cost of larger power dissipation [3]. Topology of the OTA which is used in the TIA is a gain boosted cascode amplifier.

The input transistors of the OTA have a major role in total noise of the TIA. So, utilizing long channel transistors can reduce total NF. The sensitivity of the conversion gain to the parasitic capacitors of the virtual ground in the proposed topology is much lower than that in the conventional LMV cell, due to the fact that in the proposed design the TIA is separated from the LV cell by including the mixer in between. Simulation results show a 10 MHz UGBW and 50 dB gain for the designed OTA. The resistor that is seen from virtual ground is $14 \Omega$.

It should be noted that $R_1$ and $R_2$ are assumed to be equal for proper operation of the circuit. However, $R_1$/$R_2$ unbalance results in a dc voltage offset in the virtual ground output. As the stages
The simulated IIP3 is shown in Fig. 9(a), which is equal to 13.8 kHz, because of the use of a passive mixer and series of virtual ground block. Flicker noise corner frequency is reduced by taking the mixer out of the conventional LMV cell and stacking only the two blocks of LNA and VCO, and using the mixer in current mode. Also, utilizing a passive mixer in current mode causes lower loss than a passive mixer that works in voltage mode. Simulation results show that the receiver has −7 dBm IIP3 while the receiver gain is 30 dB. Also, the quadrature oscillator differential swing is about 1.6 V peak to peak and the LO phase noise is −117 dBc/Hz at 1 MHz offset.

Thus, this paper proposes a new topology, called the LV cell, which is more suitable compared to the conventional LMV cell, for using in direct conversion receivers.

**References**


**Table 2**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>this work</th>
<th>[1]</th>
<th>[2]</th>
<th>[3]</th>
<th>[5]</th>
<th>[6]</th>
<th>[13]</th>
<th>[14]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain (dB)</td>
<td>30</td>
<td>60</td>
<td>−9.8–25.7</td>
<td>76</td>
<td>67</td>
<td>36</td>
<td>55</td>
<td>30</td>
</tr>
<tr>
<td>Power consumption (mW)</td>
<td>1.6</td>
<td>7.2</td>
<td>8.8</td>
<td>3.6</td>
<td>32.5</td>
<td>5.4</td>
<td>2.52</td>
<td>3.6</td>
</tr>
<tr>
<td>NF (dB)</td>
<td>4.7</td>
<td>8.5</td>
<td>4.4</td>
<td>9</td>
<td>16</td>
<td>4.8</td>
<td>13</td>
<td>2.5</td>
</tr>
<tr>
<td>IIP3 (dBm)</td>
<td>−7</td>
<td>N.A</td>
<td>−6.5</td>
<td>−12.5</td>
<td>−10.5</td>
<td>−19</td>
<td>−4</td>
<td>−5</td>
</tr>
<tr>
<td>Noise corner frequency (kHz)</td>
<td>−117@1 MHz</td>
<td>N.A</td>
<td>N.A</td>
<td>−116@3.5 MHz</td>
<td>−127@3 MHz</td>
<td>−104@1 MHz</td>
<td>N.A</td>
<td>N.A</td>
</tr>
<tr>
<td>(V_{dd}(V))</td>
<td>1.2</td>
<td>1.2</td>
<td>1.8</td>
<td>1.2</td>
<td>0.6</td>
<td>1.2</td>
<td>1.2</td>
<td>1.8</td>
</tr>
<tr>
<td>Technology ((\mu))</td>
<td>0.18</td>
<td>0.13</td>
<td>0.18</td>
<td>0.09</td>
<td>0.09</td>
<td>0.13</td>
<td>0.18</td>
<td>0.18</td>
</tr>
</tbody>
</table>

\(\text{TT} 27\text{C}\) \(\text{SS 70\text{C}}\) \(\text{FF \text{−40C}}\)

<table>
<thead>
<tr>
<th>TT 27 C</th>
<th>SS 70 C</th>
<th>FF −40 C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain (dB)</td>
<td>30</td>
<td>31</td>
</tr>
<tr>
<td>Power consumption (mW)</td>
<td>1.6</td>
<td>1.4</td>
</tr>
<tr>
<td>NF (dB)</td>
<td>4.7</td>
<td>7</td>
</tr>
<tr>
<td>NF corner freq (kHz)</td>
<td>14.8</td>
<td>25</td>
</tr>
<tr>
<td>IIP3 (dBm)</td>
<td>−7</td>
<td>−9</td>
</tr>
</tbody>
</table>

\(P\) in the direct conversion mode, the linearity of the receiver is calculated using tones at ±100 kHz offset from 2.4 GHz. The simulated IIP3 is shown in Fig. 9(a), which is equal to −7 dBm. The simulated input 1 dB compression point (\(P_{1\text{dB}}\)) of the receiver is −19.5 dBm (Fig. 9(b)). As shown in Fig. 9(b), the conversion gain is about 30 dB. Fig. 10 shows phase noise of the quadrature LO that is −117 dBc/Hz at 1 MHz offset frequency. The quadrature LO amplitude is 1.6 V differential swing.

**Table 3**

Simulation of process corners and temperature variations.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>TT 27 C</th>
<th>SS 70 C</th>
<th>FF −40 C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain (dB)</td>
<td>30</td>
<td>31</td>
<td>28.5</td>
</tr>
<tr>
<td>Power consumption (mW)</td>
<td>1.6</td>
<td>1.4</td>
<td>2</td>
</tr>
<tr>
<td>NF (dB)</td>
<td>4.7</td>
<td>7</td>
<td>0.5</td>
</tr>
<tr>
<td>NF corner freq (kHz)</td>
<td>14.8</td>
<td>25</td>
<td>5</td>
</tr>
<tr>
<td>IIP3 (dBm)</td>
<td>−7</td>
<td>−9</td>
<td>−10</td>
</tr>
</tbody>
</table>

\(\text{TT} 27\text{C}\) \(\text{SS 70\text{C}}\) \(\text{FF \text{−40C}}\)

following this block are most likely in differential, this common mode dc voltage will be rejected.

